IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

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| ON SEMICONDUCTOR CORP. and SEMICONDUCTOR COMPONENTS INDUSTRIES, L.L.C.,<br><br>Plaintiffs,<br><br>v.<br><br>SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG TELECOMMUNICATIONS AMERICA GENERAL, L.L.C., SAMSUNG SEMICONDUCTOR, INC., and SAMSUNG AUSTIN SEMICONDUCTOR L.L.C.,<br><br>Defendants. | C.A. No. 07-449 (JJF) |
| SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG TELECOMMUNICATIONS AMERICA GENERAL, L.L.C., SAMSUNG SEMICONDUCTOR, INC., and SAMSUNG AUSTIN SEMICONDUCTOR L.L.C.,<br><br>Plaintiffs,<br><br>v.<br><br>ON SEMICONDUCTOR CORP. and SEMICONDUCTOR COMPONENTS INDUSTRIES, L.L.C.,<br><br>Defendants. | C.A. No. 06-720 (JJF) |

**ON SEMICONDUCTOR'S OPENING CLAIM CONSTRUCTION BRIEF**

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**CASES**

## INTRODUCTION

ON Semiconductor[1] accuses Samsung[2] of infringing four ON Semiconductor patents. Three of them – U.S. Patent Nos. 5,361,001 (the "'001 patent"), 6,362,644 (the "'644 patent") and 5,563,594 (the "'594 patent") – are directed to semiconductor circuits used in electronic devices such as cellular telephones, cameras, computers, and automobiles. The fourth ON Semiconductor patent, U.S. Patent No. 5,000,827 (the "'827 patent"), as well as the one Samsung patent at issue, U.S. Patent No. 5,252,177 (the "'177 patent"), generally relate to processes for manufacturing semiconductor chips.[3] This is ON Semiconductor's opening claim construction brief in support of its constructions of the disputed claim terms of those patents.

ON Semiconductor offers constructions of the disputed claim terms that are based on their plain and ordinary meaning in the light of the intrinsic record. By contrast, Samsung's proposed constructions violate the claim construction principles set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1315-1325 (Fed. Cir. 2005) (en banc). These errors include: (1) reading limitations from dependent claims into the independent claims; (2) importing limitations from the specification; (3) construing terms to exclude described embodiments; and (4) relying on extrinsic evidence taken out of context and inconsistent with the intrinsic record to rewrite claim

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[1] "ON Semiconductor" refers collectively to ON Semiconductor Corp. and Semiconductor Components Industries, L.L.C.

[2] "Samsung" refers collectively to Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Telecommunications America General, L.L.C., Samsung Semiconductor, Inc. and Samsung Austin Semiconductor, L.L.C.

[3] For the Court's convenience, copies of each of the five patents in suit are attached hereto as Exhibits A-E. Copies of the '001, '644, '594, and '827 patents are also attached as Exhibits 1, 6, 14, and 26 to the accompanying Declaration of Richard Bauer.

language.[4] The intrinsic record, as confirmed by well established dictionaries and other scholarly references, demonstrates that ON Semiconductor's constructions are proper and should be adopted over Samsung's proposed constructions.

LEGAL STANDARD

Claim construction is a matter of law for the Court. *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 372 (1996). Because of the public notice function of the claims, "the focus is on the objective test of what one of ordinary skill in the art at the time of the invention would have understood the term to mean." *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 986 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370. To determine the meaning of a patent claim, the Court considers three sources: the claims, the specification, and the prosecution history. *Id*. at 979.

The Court looks first to the words of the claims. *Phillips*, 415 F.3d at 1312. "Although words in a claim are generally given their ordinary and customary meaning, a patentee may choose to be his own lexicographer and use terms in a manner other than their ordinary meaning, as long as the special definition of the term is clearly stated in the patent specification or file history." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). "A technical term used in a patent document is interpreted as having the meaning that it would be given by persons experienced in the field of the invention, unless it is apparent from the patent and the prosecution history that the inventor used the term with a different meaning." *Hoechst Celanese Corp. v. BP Chems. Ltd.*, 78 F.3d 1575, 1578 (Fed. Cir. 1996).

[4] *See Phillips*, 415 F.3d at 1318 ("We have viewed extrinsic evidence in general as less reliable than the patent and its prosecution history in determining how to read claim terms. . . .).

It is always necessary to review the specification to determine whether the inventor has used any terms in a manner inconsistent with their ordinary meaning. *Phillips*, 415 F.3d at 1320-1321. The specification can act as a dictionary when it expressly or impliedly defines terms used in the claims. *Id*. at 1321. Because the specification must contain a description of the invention that is clear and complete enough to enable those of ordinary skill in the art to make and use it, the specification is the single best guide to the meaning of a disputed term. Id. at 1315. When looking to the specification, however, courts must "avoid the danger of reading limitations from the specification into the claim." *Id*. 1323.

The prosecution history should also be consulted and "is often of critical significance in determining the meaning of the claims." *Vitronics*, 90 F.3d at 1582. Disputed claim terms are construed consistently across all claims within a patent. *Southwall Techs. v. Cardinal IG.*, 54 F.3d 1570, 1579 (Fed. Cir. 1995).

Extrinsic evidence should be used only if needed to assist in determining the meaning or scope of technical terms in the claims, and may not be used to vary or contradict the terms of the claims. *Phillips*, 415 F.3d at 1322. The Court is free to consult technical treatises and dictionaries, however, to better understand the underlying technology and to rely on dictionary definitions when construing claim terms, so long as they do not contradict any definition found in, or ascertained by, a reading of the patent documents. *Id*.

Whether to treat a preamble as a limitation is a determination "resolved only on review of the entirety of the patent to gain an understanding of what the inventors actually invented and intended to encompass by the claim." *Corning Glass Works v. Sumitomo Elec. U.S.A., Inc.*, 868 F.2d 1251, 1257 (Fed. Cir. 1989). In general, a preamble limits the claimed invention if it recites essential structure or steps, or if it is "necessary to give life, meaning, and vitality" to the claim.

*Catalina Mktg. Int'l v. Coolsavings.com, Inc.*, 289 F.3d 801, 808, (Fed. Cir. 2002) (quoting *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1305 (Fed. Cir. 1999)). If the body of the claim fully and intrinsically sets forth the complete invention, including all of its limitations, and the preamble merely states, for example, the purpose or intended use of the invention, then it is of no significance to claim construction because it cannot be said to constitute or explain a claim limitation. *Pitney Bowes*, 182 F.3d at 1305; *see also Rowe v. Dror*, 112 F.3d 473, 478 (Fed. Cir. 1997); *Allen Eng'g Corp. v. Bartell Indus.*, 299 F.3d 1336, 1346 (Fed. Cir. 2002) ("Generally, the preamble does not limit the claims.").

## ARGUMENT

### I. U.S. PATENT NO. 5,361,001

#### A. Introduction to the Claims

Claim 4 is being asserted in the present litigation:[5]

> 4. A method of ***analog trimming***, comprising the steps of:
> enabling conduction through a passive element in response to a first state of a ***control signal***;
> disabling conduction through said passive element in response to a second state of said ***control signal***;
> activating said ***control signal*** in response to a data signal to enable and disable said conduction through said passive element, said activating step including the steps
> (a) latching said data signal, and
> (b) logically combining said data signal with a logic signal for providing said ***control signal***; and
> ***setting said control signal to a fixed value*** after removal of said data signal.

[ Ex. 1, Col. 5:27-6:7.][6]

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[5] Emphasis in the quoted material is added unless otherwise noted.

[6] "Ex. _____" refers to the numbered exhibits attached to the accompanying Declaration of Richard J. Bauer.

The ’001 patent is generally directed to methods for performing analog trimming. [*Id*., Col. 1:6-10.] The use of the term “trimming” in the ’001 patent relates to tuning or adjusting analog values in a circuit to get them just right for a particular application. [*Id*., Col. 1:21-24.] Although electronic components are generally made uniformly, trimming is necessary because the manufacturing process introduces some variation in the electrical characteristics of each individual device. [*Id.,* Col. 1:10-23 (“To compensate for the process variability, many electronic circuits use analog trimming during test to set resistor values as necessary for proper operation of the circuit.”)] The ’001 patent teaches incorporating multiple analog components, resistors for example, than can be individually turned on and off to create a specific analog value to correct for this variation, or to optimize the component for a particular application. [*Id., C*ol. 2:15-45.]

To test the trim amount before applying it, the inventors of the ’001 patent devised a method by which they could “preview” the trimming until they got it right. [*Id.*, Col. 1:6-10.] Once the trim value was chosen appropriately, it could be “fixed” for a particular circuit. [*Id.*, Col. 4:14-17.] In this way, the circuit could be customized for a particular application.

For example, Figure 1 of the ’001 patent shows a series of resistors (resistors 12, 14, 16, and 18) that affect the total resistance from point 19 to point 20. [*Id.*, Col. 2:15-18.] Any one or more of these resistors can be “enabled or disabled” by controlling the corresponding transistor (transistors 26, 30, and 34, respectively). [*Id*., Col. 2:28-45.] By inputting the appropriate information (DATA) to the CONTROL CIRCUITS, different combinations can be

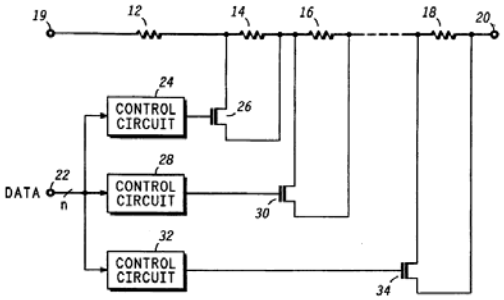


FIG. 1

explored (i.e., "previewed"). [*Id*. Col. 2:37-42.] Once the right combination is found, the control signals to the transistors can be fixed. [*Id*., Col. 4:14-17.]

B. The Disputed Claim Construction Issues

1. "Analog Trimming"

| **ON Semiconductor** | **Samsung** |
|---|---|
| *This term appears only in the preamble and is not a claim limitation and therefore does not require construction.*<br><br>*If the Court is inclined to construe this term, it should be construed as follows:*<br><br>modifying an analog value or quantity | *The preamble is a limitation and should be construed as follows:*<br><br>making fine adjustments of capacitance, inductance, or resistance of an analog component. |

a. This Term From the Preamble Does Not Require Construction

The claim phrase "analog trimming" in the preamble is not a limitation because it neither recites essential structure or steps nor is it necessary to give "life, meaning, and vitality" to the claim. *Pitney Bowes*, 182 F.3d at 1305. The preamble does not recite essential steps because the body of the claim fully and intrinsically sets forth the complete invention, including all of its limitations. Aside from the preamble, no further reference is made anywhere in the body of the claim to "analog trimming." This statement of purpose or intended use is not sufficient to make the preamble a claim limitation. *Catalina Mktg.*, 289 F.3d at 808. There also is no evidence from the prosecution history where the '001 inventor distinguished the prior art based on the phrase "analog trimming." Therefore, the preamble phrase "analog trimming" requires no construction.

b. If This Term Requires Construction, It Should Be Construed to Mean "Modifying an Analog Value or Quantity"

If the Court concludes that the term "analog trimming" should be construed, the term should be given its plain and ordinary meaning. The plain meaning of "trimming" is "modifying." [Ex. 2 at 1259 (defining the term "trimming" as "to adjust to a desired position").] Therefore, the plain meaning of the phrase "analog trimming" would be "modifying an analog value or quantity."

The specification supports this plain meaning. It states that "[t]he trimming is temporary and may be modified with different data signals to achieve optimal results." [Ex. 1, Col. 4:35-37.] When discussing a particular example of "analog trimming," the specification explains that "[t]he resistor ladder should be adjustable at wafer test over a range from say 10 to 2,560 ohms in 10 ohm increments," where resistance is an analog quantity or value. [*Id*., Col. 1:36-38.] Thus, the term "analog trimming" is used in the specification to refer to adjusting an analog value or quantity, including resistors, capacitors, transistors, voltages, frequencies, and gain [*Id*. at 1:12-20.] There is no mention or discussion of the phrase "analog trimming" in the prosecution history.

In addition to the intrinsic evidence, extrinsic evidence also supports ON Semiconductor's interpretation. For example, consistent with the discussion above, the Modern Dictionary of Electronics defines "analog" as "[t]he representation of numerical quantities by means of physical variables, e.g., translation, rotation, voltage, resistance." [Ex. 3 at 39-40.]7

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7 The Court may rely on dictionary definitions when construing claim terms, so long as they do not contradict any definition found in or ascertained by a reading of the patent documents. *Phillips*, 415 F.3d at 1318. Here, contemporaneous references are consistent with the inventors' use of the term in the specification.

The Merriam-Webster's Collegiate Dictionary describes "trim" as "to adjust to a desired position." [Ex. 2 at 1258.] Another reference discusses that "[t]he precision of many analog CMOS circuits depends on the matching of MOS transistors" and that "[i]f the required accuracy cannot be achieved by this technique, trimming may help further." [Ex. 4 at 1437-1440.] These statements relate to modifying certain transistor parameters (analog values). The authors' description of certain known trimming techniques, including "laser trimming, programming of resistor networks (e.g., by Zener zapping [2] or fusible links [3]), and dynamic compensation," is significant because some of these techniques are mentioned in the '001 patent. [*See, e.g.*, Ex. 1, Col. 1:42-43, 1:48-52, and 2:15-18.]

Samsung agrees that "trimming" relates to "adjusting," but then improperly seeks to add additional limitations that are inconsistent with the plain meaning of this phrase and the intrinsic evidence. For instance, Samsung's proposed construction would require the "making of a fine adjustment." [D.I. 117 at 8.][8] Not only is this "fine" limitation found nowhere in the claim, specification, or the file history, but the patent teaches a ***large*** (not a "fine") range of adjustments from 10 to 2,560 ohms. [Ex. 1, Col. 1:36-38.] Samsung attempts to narrow this limitation even further by proposing to limit the "fine adjustment" to "capacitance, inductance, or resistance." Although these examples are analog quantities or values, they are in no way an exhaustive list. In fact, the specification mentions additional analog values, including voltage, frequency, and gain. [*See, e.g.*, Ex. 1, Col. 1:12-20.] Samsung's proposed construction goes even farther astray, proposing that the term "analog trimming" somehow references an "analog circuit component."

[8] For simplicity, all citations to the record refer to docket entries in C.A. No. 06-720-JJF unless otherwise specified.

There is, however, no support for adding a circuit limitation to the simple term "analog trimming."

2. "Control Signal"

| ON Semiconductor | Samsung |
|---|---|
| a signal that conveys information about regulation or guidance | a signal that enables or disables conduction through an associated passive element |

Samsung appears to contend that "signal" need not be construed because it uses the term "signal" in its construction of "control signal." To narrow the issues for the Court, ON Semiconductor accepts Samsung's position and also includes the word "signal" as part of its construction.[9] The remaining issue here is to determine what "control" means.

The plain meaning of the term "control signal" is a signal that provides control. The term is consistently used in this manner throughout the claims, the specification, and the prosecution history. To provide guidance to the jury, ON Semiconductor proposes that "control signal" be expanded to "a signal that conveys information about regulation or guidance" because "control" in the '001 patent relates to regulation or guidance.

Claim 1 itself explains the function of the control signal: "a control signal for enabling and disabling conduction through said passive element." As stated here, "control signal" conveys information about the regulation of conduction through the passive elements. More specifically, the control signal regulates when the passive elements are to be turned on (enable conduction) or off (disable conduction). ON Semiconductor's construction is fully consistent with this usage and the usage of the term in other claims. [*See, e.g.*, Ex. 1, Col. 6:4-5 (claiming "logically combining said data signal with a logic signal for providing said control signal").] *Phillips*, 415 F.3d at 1314 (explaining that "the context in which a term is used in the asserted

[9] ON Semiconductor does similarly for other terms involving signal, including "clock signal," "transfer data signal," and "termination signal" as discussed further below.

claim can be highly instructive" as well as "[o]ther claims . . . , both asserted and unasserted, can [ ] be valuable sources of enlightenment as to the meaning of a claim term").

Similarly, the specification states that "[c]ontrol circuit 24 provides a control signal to the gate of MOS transistor 26." [Ex. 1, Col. 2:28-29.] This passage explains that the control signal applies a signal to the gate of MOS transistor so as to regulate or guide its operation; in essence the control signal is turning MOS transistor 26 on and off. Other passages of the specification discuss control signals regulating the operation of MOS transistors 30 and 34. [*See, e.g.*, Ex. 1, Col. 2:31-35.] Nothing in the prosecution history contradicts this construction. [*See* Ex. 5.]

Extrinsic evidence further confirms that ON Semiconductor's construction is correct. For example, Merriam-Webster's Collegiate Dictionary defines "control" as "to exercise restraining or directing influence over: regulate." [Ex. 2 at 252.] Similarly, the IEEE Standard Dictionary of Electrical and Electronics Terms defines it as "[b]roadly, the methods and means of governing the performance of any electric apparatus, machine, or system." [Ex. 34, p. 133.] *See Phillips*, 415 F.3d at 1318 ("[D]ictionaries, and especially technical dictionaries, endeavor to collect the accepted meanings of terms used in various fields of science and technology," and so "those resources have been properly recognized as among the many tools that can assist the court in determining the meaning of particular terminology to those of skill in the art of the invention.") Eschewing this plain meaning, Samsung proposes that "control" should mean "enable or disable conduction through an associated passive element of a trim circuit." That construction, however, not only reads in other limitations from other claim elements (e.g., enable/disable conduction) but also reads in limitations from the specification (e.g., trim circuit), which is improper. [*See, e.g.*, Ex. 1, Abstract; Col. 1:6-9; 2:15-18.] *See Phillips*, 415 F.3d at 1323 ("[A]lthough the specification often describes very specific embodiments of the invention, we have repeatedly

warned against confining claims to those embodiments."); *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1119 (Fed. Cir. 2004) (rejecting proposed construction that "largely read[ ] the term 'operatively' out of the phrase 'operatively connected,'" finding "[w]hile not an absolute rule, all claim terms are presumed to have meaning in a claim.").

The same term, "control signal," is also disputed in the '594 patent. Because "control signal" is a well-understood term with no special meaning in either patent, ON Semiconductor proposes identical constructions for both; Samsung's are drastically different. *See Phillips*, 415 F.3d at 1314 (finding involves little more than the application of the widely accepted meaning of commonly understood words). For example, as discussed below, for the '594 patent, Samsung proposes that "control signal" should mean "a signal for controlling the phase of the transfer data signal." Samsung's proposed constructions are improper in both instances and should be rejected.

3. "Fixed Value"

| **ON Semiconductor** | **Samsung** |
|---|---|
| a state that is not fluctuating or varying during a specified or predetermined time or condition | a value that does not change |

The terms "fixed" and "value" are familiar and the concept of "fixed value" is also well-known to one skilled in the art. ON Semiconductor's proposed definition is based on the well-understood and plain meaning of this phrase.

In ordinary usage, "fixed" does not necessarily mean "the same forever." A fixed price contract, for example, eventually expires and a new price may be negotiated for the next fixed price contract. Likewise, even a fixed time for a meeting may be changed to a new fixed time. When used in its ordinary sense, the term "fixed value" can be understood to relate to a state that is not fluctuating or varying, but that can change from time to time or according to changed

conditions. Accordingly, "fixed value" should be construed as "a state that is not fluctuating or varying during a specified or predetermined time or condition."

The claims' usage of "fixed value" is consistent. For example, claim 4 recites "setting said control signal to a fixed value." [*See* Ex. 1, Col. 6:6.] This phrase can be understood to mean that the control signal is to be set to a particular state or condition. Nothing in the claim language says that the value, once set, can not be changed again. In contrast to claim 1, dependent claim 5 recites "blowing a fuse to set said control signal at said fixed value." Once a fuse is blown, it cannot be easily restored to its previous state – it is essentially an extremely fixed value. [Ex. 1, Col. 4:9-14.] If setting the value in claim 1 were intended to be permanent, claim 5 would be redundant and add no further limitation to the independent claim. *Free Motion Fitness, Inc. v. Cybex Int'l*, 423 F.3d 1343, 1351 (Fed. Cir. 2005) (A "difference in meaning and scope between claims is presumed to be significant 'to the extent that the absence of such difference in meaning and scope would make a claim superfluous'") (quoting *Tandon Corp. v. U.S. Int'l Trade Comm'n*, 831 F.2d 1017, 1023 (Fed. Cir. 1987)); *Nazomi Commc'ns, Inc. v. Arm Holdings, PLC.*, 403 F.3d 1364, 1370 (Fed. Cir. 2005) ("Claim differentiation 'normally means that limitations stated in dependent claims are not to be read into the independent claim from which they depend."). Reference to extrinsic evidence further confirms this construction. For example, a definition for "fixed logic levels" as "[d]igital data with high and low levels that are programmable or adjustable" demonstrates that these levels are fixed, or set, but can be adjusted at different times or for different conditions. [Ex. 3 at 380-381.]

Not surprisingly, Samsung's construction attempts to narrow the term's ordinary meaning. By proposing that "fixed value" should be "a value that does not change," Samsung proposes that the term should mean "permanent and never changing." (*See also* Samsung's

proposed construction for "setting said control signal to a fixed value," i.e., "permanently setting the state of the control signal.") Samsung appears to base its construction on an example given in the specification that a fixed value can be achieved by blowing a fuse, which is actually part of dependent claim 5 (discussed above). [*See, e.g.*, Ex. 1, Col. 6:8-12.] Samsung ignores, however, that the specification does not indicate that this was the only manner of setting a fixed value. *See Acumed LLC v. Stryker Corp.*, 483 F.3d 800, 808 (Fed. Cir. 2007) ("limitations from the specification are not to be read into the claims"). Indeed, it describes other conditions in which a value is set, such as latch circuits that can hold data and keep it from fluctuating for predetermined times or conditions but can be changed or reset. [*See, e.g.*, Ex. 1, Col. 2:49-52.] Moreover, the registers described for the '594 patent can also hold data and keep it from fluctuating for certain times or conditions but can be reset to other values at a later time. [*See* Ex. 14, Col. 1:6-60.] Most importantly, there is nothing in the intrinsic evidence that indicates that the inventor was acting as his own lexicographer to re-define an otherwise well-understood term. Indeed, because it is so well-understood, the burden on Samsung is high to demonstrate a deviance from its well understood meaning. *See, e.g., Abraxis Bioscience, Inc. v. Mayne Pharma Inc.*, 467 F.3d 1370, 1376 (Fed. Cir. 2006) (a patentee may "act as his own lexicographer," but must do so clearly "to specifically define terms of a claim contrary to their ordinary meaning") (citing *Chef Am., Inc., v. Lamb-Weston, Inc.*, 358 F.3d 1371, 1374 (Fed. Cir. 2004)).

4. "Setting Said Control Signal to a Fixed Value"

| **ON Semiconductor** | **Samsung** |
|---|---|
| *The Court need not construe this, however, if the Court is inclined to construe this, ON Semiconductor contends that the phrase can be understood with the following constructions:*<br><br>fixed value – separately construed (discussed separately above) | Permanently setting the state of the control signal<br><br>*Samsung also proposes the following constructions:*<br><br>fixed value - Permanently setting the state of the control signal (discussed separately above) |

| | |
|---|---|
| control signal – separately construed (discussed separately above) | control signal - A signal that enables or disables conduction through an associated passive element of a trim circuit (discussed separately above) |

Having separately construed the terms "control signal" and "fixed value" and because there is no dispute with the term "setting," there is nothing more to construe here. As discussed above, Samsung should not be permitted to import narrowing limitations into the claims.

II. U.S. PATENT NO. 6,362,644

A. Introduction

Independent claim 6 of the '644 patent is exemplary and recites:

> 6. An integrated circuit, comprising:
> a semiconductor package having
> first and second ***pins*** respectively adapted for receiving first and second data signals,
> ***third and fourth pins for respectively receiving first and second termination signals***, and
> a supply pin ***coupled*** for receiving a power supply voltage; and
> a semiconductor die housed in the semiconductor package for operating from the power supply voltage, and
> having a first ***load element*** coupled between the first and third ***pins*** to ***terminate*** the first data signal, and
> a second ***load element*** coupled between the second and fourth ***pins*** to ***terminate*** the second data signal.

[Ex. 6, Col. 5:56-6:10.]

The general problem addressed in the '644 patent is analogous to that of echoes in a cavernous room. Where a speaker may be trying to convey an important message to a listener across the room, undesirable echoes may make it difficult, if not impossible, to receive the proper message. Indeed, the echoes may even confuse the speaker.

A similar thing can happen in an electrical circuit. When sending a fast electrical signal from a driver circuit (e.g., "speaker") to a receiver circuit (e.g., "listener") over relatively long distances along a wire (e.g., "large room"), these electrical signals can bounce back (i.e., be

reflected) in a way analogous to an echo. In this undesirable situation, the receiver circuit may not understand or receive the correct information, which can cause problems with the entire circuit. Also, the reflected signals can cause problems with the driver or sending circuit.

Just as a room can be acoustically improved to deaden undesirable echoes (for example, with acoustic ceilings or walls), a wire carrying data susceptible to reflections can be "terminated," often times with a resistor as a load element connected to a power supply to achieve the same results electrically. [*See, e.g.*, Ex. 6, Col. 1:21-23.] The '644 patent further provides for programmable terminations that can accommodate different requirements (for example, integrated circuits operating under different conditions). [Ex. 6, Col. 1:67-2:2, 2:20-23.]

Figure 5 of the '644 patent describes a termination scheme in which load elements (e.g., terminating resistors 108 and 110) residing on a chip 96 (also called a semiconductor die) are connected at one end to power supplies (e.g., VB and VA, respectively) and to data inputs (e.g., IN2 119 and IN1, respectively). [*See* Ex. 6, Col. 4:16-45.] The semiconductor die 96 is further described as housed within a semiconductor package 90 having various pins (e.g., 97, 99, 117, and 119). [Ex. 6, Col. 4:16-27.]

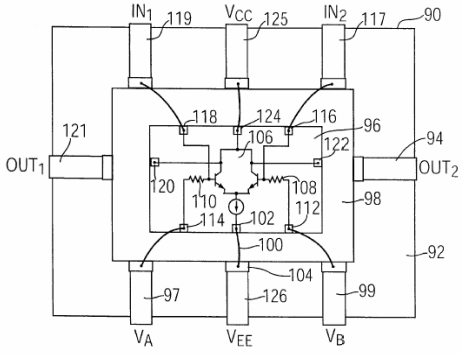


FIG. 5

B. The Disputed Claim Construction Issues

1. "Terminate," "Termination signal," "Load Elements," and "Loading"

To properly understand the terms "terminate," "termination signal," "load elements," and loading," it is helpful to have a further foundation on the termination of a circuit.

a. Background on Transmission Lines and Their Termination

Modern digital circuitry operates at very high speeds. This digital circuitry, although representing digital information as 1's and 0's, actually operates by changing voltages over time. [*See* Ex. 7 at 397.] To represent a logic level 1 in a data bus, for example, a digital circuit may switch a transistor to provide 1.8 volts on the bus. And to later represent a logic level 0, the same transistor may be switched to provide 0 volts. Although the final voltage values are interpreted by the circuits as either a "1" or a "0," the change is not instantaneous and takes time to go from "1" down to "0" or vice versa. [*Id*. at 397, 399-400.]

In rapidly changing voltage levels, complex electrical signals are generated that are much more complicated than the often-shown, simplified square waves of digital circuitry. Close examination of the signals reveals that there may be complex "ringing" within the signal. [*Id*. at 399-400.] If this ringing is not properly controlled, signals can be reflected along a wire (sometimes referred to as a transmission line) and cause undesirable effects. [*Id*.]

On a data bus transmission line, this type of reflection can cause troublesome interference, drastically affecting the information desired to be conveyed. [*Id.* at 398.] For example, where a logic level 1 is to be transmitted, the reflections may cause a logic level 0 to be read, or vice versa. In still other situations, the reflections may cause a circuit to be completely inoperable.

To eliminate the reflection of unwanted signals, a transmission line, such as a wire or conductive path in a memory circuit, is often terminated by providing a load element (sometimes called just a "load") connected to a power supply that then dissipates the unwanted signal. [*See*, *e.g.*, Ex. 8 at 12; Ex. 9 at 23.] The specification of the '644 patent describes the connection of the load element to the power supply as termination signals. [Ex. 6, Col. 4:49-54.] Moreover, it

explains that the load element may be a resistor, among other things. [Ex. 6, Col. 1:24-27, 2:18-20.] As a consequence of the physics involved, an ideal termination is a load that equals the impedance of the transmission line. [*See* Ex. 6, Col. 1:24-29; Ex. 7 at 397-408.] In the real world however, ideal termination is not always possible. But even if the termination is not exactly equal or if the impedance of the transmission line is only known approximately, some termination is better than no termination. [*See* Ex. 6, Col. 1:24-26.]

(i) "Terminate"

| **ON Semiconductor** | **Samsung** |
|---|---|
| to dissipate or absorb energy | The use of a load at the end of a transmission line or other device whose impedance is matched to that of the line |

One of ordinary skill in the art would read the claims of the '644 patent in the context of the need for proper termination of electrical signals as generally discussed above. *See CVI/Beta Ventures, Inc. v. Tura LP*, 112 F.3d 1146, 1160 (Fed. Cir. 1997) (explaining claims are construed in light of "the problem the inventor was attempting to solve" and in a manner that "is consistent with and furthers the purpose of the invention"), *cited with approval in Phillips*, 415 F.3d at 1314. The claims of the '644 are consistent with this understanding, as are the specification and the prosecution history. Samsung's construction is improperly narrow and should be rejected.

To terminate a transmission line is to dissipate or absorb unwanted energy on the transmission line so as to prevent reflection by absorbing undesirable signals. Asserted claim 6 demonstrates a consistent usage in reciting "termination signals" that can be power supply voltages as described in the specification. [Ex. 6, Col. 4:46-54.] Moreover, claim 6 recites the termination of data signals ("terminate the first/second data signal") to avoid unwanted reflections. Importantly, there is nothing in the other limitations of claim 6 that narrows a termination to an idealized termination equaling the impedance of a transmission line. All that is

recited is that the termination be provided by a load element (claim 6) that may be a resistor (*e.g.*, dependent claim 7), but no mention is made that they must be of idealized values.

The specification is fully consistent with this interpretation. It makes clear that not all terminations are chosen to be equal to the impedance of the transmission line: "[t]he resistance is typically chosen to equal the impedance of the interconnect transmission line to help reduce interconnect signal distortion." [Ex. 6, Col. 1:23-27.] Likewise, notwithstanding extensive discussion in the patent prosecution history about the invention and certain prior art references as they relate to termination, the inventors never attempted to limit a termination load to an idealized value. Their usage of the term was consistent with their usage in the specification and the claims and with the understanding of one of ordinary skill in the art.

Samsung argues that "terminate" means "the use of a load at the end of a transmission line or other device whose impedance is matched to that of the line." Thus, Samsung is attempting to limit any "termination" to an idealized situation by first describing "the use of a load at the end of a transmission line or other device" and then limiting its application to where the impedance of the load is "matched to that of the line." This directly contradicts the inventors' teaching that not all terminations are ideal. [Ex. 6, Col. 1:23-27.] Samsung's proposed construction contradicts the specification and the teaching of the patent, and should be rejected.

(ii) "Termination Signal"

| **ON Semiconductor** | **Samsung** |
|---|---|
| a signal that dissipates or absorbs energy | A signal that configures the circuit to receive data signals from one of several available logic families |

With an understanding of "terminate," as discussed above, "termination signal" is readily understood, especially since there is no dispute about the meaning of "signal." For that reason,

ON Semiconductor refers back to the meaning of "terminate" for its construction of "termination signal": "a signal that dissipates or absorbs energy."

The intrinsic evidence with regard to "terminate" similarly applies to this term. Moreover, the specification of the '644 patent describes that "FIG. 1 has external (configuration) termination pins 22, 24 which are configured to receive different termination signals depending on the logic family application." [Ex. 6., Col. 4:49-52.] The described embodiment is adaptable to operate with different types of circuitry such as circuitry operating at different voltages or different speeds. [*See* Ex. 6, Col. 2:25-33.] But the asserted claims are not limited to these aspects of the described embodiments.

Separately, the '644 patent describes that pins 22 and 24 respectively correspond to certain predetermined voltages, VA and VB. [Ex. 6, Col. 2:25-33.] As discussed above, a termination, such as a resistor, must be connected to a power supply to properly dissipate the unwanted signals. Moreover, the specification of the '644 patent explains that certain types of signals should be terminated using particular voltage signals, e.g., termination signals. [*See* Ex. 6, Col. 2:25-33.] Applicants' comments during prosecution are similarly consistent. [*See* Ex. 10, at 10-13 "the Kubista termination network is suitable for terminating differential signals, but does not have the flexibility of the claimed invention in terminating signals from a variety of logic families, depending on the value of the first and second termination signal".]

By contrast, Samsung proposes an improperly narrow construction that must be rejected. Despite that independent claim 6 makes no mention of logic families, Samsung improperly attempts to import limitations from the dependent claims (e.g., dependent claims 10 and 11) or the specification both of which are improper. [*See, e.g.*, Ex. 6, Col. 1:67-2:2.] *See Phillips*, 415 F.3d at 1315 (instructing that "the presence of a dependent claim that adds a particular limitation

gives rise to a presumption that the limitation in question is not present in the independent claim."); *Free Motion Fitness*. 423 F.3d at 1351. Proposing that the termination signal is "a signal that configures a circuit to receive data signals" is yet another attempt to read in limitations from the specification that should be rejected. [*See* Ex. 6, Col. 4:49-62.] *See Phillips*, 415 F.3d at 1323 (cautioning against importing limitations from the specification into the claims).

b. "Load Elements"

| **ON Semiconductor** | **Samsung** |
|---|---|
| electrical devices capable of dissipating or absorbing electrical energy | An impedance that provides a termination for a logic device transmission line to help reduce interconnect signal distortion |

As discussed above in the background section, a load element is an electrical device, such as a resistor, that acts in conjunction with a power supply voltage to dissipate unwanted or spurious signals. ON Semiconductor's construction includes the aspects understood by one of ordinary skill in the art.

The discussion of "terminate" and "termination signal" above is closely related to "load elements" because it is the load elements that operate in conjunction with the terminating signal to dissipate unwanted signals. The same intrinsic evidence supports ON Semiconductor's construction here. Moreover, the claims make clear that "load elements" (*see* claim 6) may include resistors (*see* claim 7), but also may include other things, such as capacitors or inductors. [*See* Ex. 11 at 389 (defining the term "loading" as "[t]he matching of source impedance to load impedance, usually by means of the introduction of an inductance or capacitance into the load itself").]

Samsung's construction, not atypically, is improperly narrow. For example, Samsung's construction includes "interconnect signal distortion." Samsung reads in this language from the background section of the '644 patent that describes a narrow condition. [Ex. 6, Col. 1:27-29.]

Nothing in the patent, however, limits the claim to dealings only with this condition. Samsung also reads in a "logic device" from the background section of the specification. [*See* Ex. 6, Col. 1:8-20.] A "load element" has much broader application, as discussed above, and there is nothing about the term "load elements" that restricts it to a "logic device transmission line."

c. "Loading"

| **ON Semiconductor** | **Samsung** |
|---|---|
| applying effects that dissipate or absorb electrical energy | Placing an impedance at the end of a transmission line or other device to match that of the line |

"Loading" is closely related to the above discussed "load element" term. As taught by the '644 patent, "loading" is achieved by applying "load elements." [*See, e.g.*, Ex. 6, Col. 3:16-20.] The two terms should be construed consistently. The above-cited intrinsic evidence relating to "terminate," "termination signal," and "load element" likewise support ON Semiconductor's construction . The discussion of "terminate" is particularly relevant since termination is achieved by loading a transmission line.

Samsung offers an overly narrow construction that seeks to include a limitation requiring a matched impedance of the transmission line into this term also. As discussed with reference to "terminate," this contradicts the specification that contemplates terminations that are not always matched. [Ex. 6, Col. 1:21-27.] Samsung's proposed construction should be rejected here also.

2. "Pins"

| **ON Semiconductor** | **Samsung** |
|---|---|
| a conductor configured to make an electrical connection | A small diameter metal rod used as an electrical terminal external to the semiconductor package housing |

In semiconductor devices, connections to the outside world are made through pins. [*See* Ex. 6, Col. 2:20-28.] ON Semiconductor's construction recognizes the full scope of this term whereas Samsung's construction is too narrow and contradicts the intrinsic evidence.

The claims use the term "pin" as it is understood by one of ordinary skill in the art with no notable limitations. Also, in the specification, the inventors used the term pin to refer to certain conductors configured to make electrical connections. [*See, e.g.*, Ex. 6, Col. 2:16-44.] Moreover, the inventors provided figures that include pins (*see, e.g.*, Fig. 5, reference numbers 94, 97, 99, 117, 119, 121, 125, and 126) but that do not depict the "small diameter metal rods" suggested by Samsung. The inventor's depiction of pins is shown as rectangular connections rather than metal rods. Thus, under Samsung's proposed construction, the claim would exclude even the preferred embodiment. *Oatey Co. v. IPS Corp.*, 514 F.3d 1271, 1276 (Fed. Cir. 2008) ("We normally do not interpret claim terms in a way that excludes embodiments disclosed in the specification."); *MBO Labs., Inc. v. Becton, Dickinson & Co.*, 474 F.3d 1323, 1333 (Fed. Cir. 2007) ("[A] claim interpretation that excludes a preferred embodiment from the scope of the claim is rarely, if ever, correct.").

ON Semiconductor's construction is consistent with the specification and industry usage of the term. A "pin" can refer to different kinds of conductive structures configured to make an electrical connection, including metal pads, conductive tabs, or metallized balls. For example, integrated circuits may include metal tabs, also called pins, that extend from the package and are used for affixing to a receptacle on a circuit board. [*See* Ex. 12 at 3, 16-18 (note pins are described on pg. 3 but only edge-type connectors are shown in the package drawings of pp. 16-18).] Still other types of packages include balls on the underside of a package that are then pressed onto a circuit board so as to make a connection. Samsung itself calls these balls "pins" despite the fact that they are not small diameter metal rods. [*See, e.g.*, Ex. 13, p. 3 (describes the pinout for a 60 ball FBGA (Fine-pitch Ball Grid Array; also note "Pins B3 and A2 have identical capacitance as pins B7 and A8").)] In fact, certain standards setting bodies, including JEDEC,

also call these balls pins. [*See*, *e.g.*, Ex. 9 at 12 ("NOTE 2 Pins B3 and A2 have identical capacitances as pins B7 and A8."), 20 ("The ODT pin [ball K9 of pg. 12] will be ignored if the EMR(1) is programmed to disable ODT.").] The only common feature of all of these connectors called pins is that they are conductors that provide an electrical connection as construed by ON Semiconductor.

3. "Third and Fourth Pins for Respectively Receiving First and Second Termination Signals"

| **ON Semiconductor** | **Samsung** |
|---|---|
| *The Court need not construe this, however, if the Court is inclined to construe this, ON Semiconductor contends that the phrase can be understood with the following constructions:* | Third and fourth pins that receive different termination signals (e.g., not power supply or ground pins) dependant upon the selected one of several available logic families.<br><br>*Samsung also proposes the following constructions:* |
| pins - a conductor configured to make an electrical connection (discussed separately above) | pins - A small diameter metal rod used as an electrical terminal external to the semiconductor package housing (discussed separately above) |
| termination signals - an electrical effect that terminates (discussed separately above) | termination signals - A signal that configures the circuit to receive data signals from one of several available logic families (discussed separately above) |

Having already discussed the meaning of "pins" and "termination signals," there is nothing further to construe here. The larger phrase is readily understood with an understanding of its constituent terms.

Samsung denies that this phrase can be understood for the sole purpose of seeking to rewrite it. Samsung goes so far as to propose a construction with negative limitations about power supply or ground pins despite the fact that a termination is typically made to a power supply. There is nothing in the claims that restricts this phrase in such a manner. Samsung once again attempts to read in aspects of the dependent claims (claims 10 and 11) and the specification

relating to logic families which is improper. [*See, e.g.*, Ex. 6, Col. 1:67-2:12, 6:21-28 (claims 10 and 110).] *Phillips*, 415 F.3d at 1323.

4. "Coupled"

| **ON Semiconductor** | **Samsung** |
|---|---|
| linked together | *The meaning of this term requires no construction. To the extent a construction is necessary, the term should be construed as* directly connected |

The term "coupled" appears in both the '644 and the '594 Patents. This is a very common term in electrical and electronic patents and is used in these patents according to its plain and ordinary meaning exactly as construed by ON Semiconductor.

The coupling of circuit components can occur in several ways; it can be achieved by capacitive or inductive coupling or by a direct connection, to name a few. Technical dictionaries further illustrate that "coupling" is understood by those of ordinary skill in the art to be broader than a direct connection. For example, the Modern Dictionary of Electronics defines "coupling" as "[a] mutual relation between two circuits that permits energy transfer from one to the other." [Ex. 3, pp. 208-209.] It further clarifies that "[c]oupling may be direct through a wire, resistive through a resistor, inductive through a transformer or choke, or capacitive through a capacitor." It further demonstrates that although a "coupling may be a direct wire" (i.e., a "direct connection"), it also can include capacitive or inductive coupling.

No direct connection is made but the physics of electrical signals is utilized to link different parts of a circuit. Likewise, the '644 patent is not limited to couplings that are direct connections. There is no evidence that the inventors acted as their own lexicographers to re-define an otherwise well understood term. *Vitronics*, 90 F.3d at 1582.

5. "Programmable Termination"

| ON Semiconductor | Samsung |
|---|---|
| an electrical circuit that can be configured to provide various levels or degrees for the dissipation or absorption of electrical energy | The capability to configure the circuit to receive data signals from one of several available logic families |

The above sections on termination and the related termination terms (e.g., "terminate" and "terminating signal," "load element," and "loading") apply here. From such discussion, it is understood that "termination" relates to the "dissipation or absorption of electrical energy." The only task left is to determine how "programmable" modifies "termination."

From its usage in the claims (e.g., claim 12) one of ordinary skill in the art would understand that the plain meaning of a "programmable termination" relates to a termination that can be programmed, that is, that can be configured in different ways. The specification clarifies that the inventors contemplated that a "programmable termination" could be configured so as to meet the needs of different types of circuitry, such as from different logic families. [Ex. 6, Col. 1:64-2:2, 2:20-33.] But nothing in the specification or the claims limits programmability to the selection of a logic family.

Reference to extrinsic evidence confirms this plain meaning. The Modern Dictionary of Electronics defines "programmable" as "[t]hat characteristic of a device that makes it capable of accepting data to alter the state of its internal circuitry to perform two or more specific tasks." [Ex. 3, pp. 782-785.] This is entirely consistent with the construction that an electrical circuit that can be "configured" in different ways.

Samsung's proposed construction attempts to read in limitations from the dependent claims (*see, e.g.*, claim 14) or the specification that address logic families. [Ex. 6, Col. 1:64-2:2, 2:20-33, 6:44-48 (claim 14).] Nothing suggests, however, that the claims are so limited. Samsung's attempt to read in these limitations is improper and should be rejected. *See Phillips*, 415 F.3d at 1323.

6. "First and Second Load Elements Are Coupled to Third and Fourth Pins of the Semiconductor Package to Provide a Programmable Termination"

| **ON Semiconductor** | **Samsung** |
|---|---|
| *The Court need not construe this, however, if the Court is inclined to construe this, ON Semiconductor contends that the phrase can be understood with the following constructions:* | The first and second load elements are connected to the third and fourth pins that receive different signals to configure the circuit to receive data signals from one of several available logic families<br><br>*Samsung also proposes the following constructions:* |
| load elements - electrical devices capable of dissipating electrical energy (discussed separately above) | load elements - An impedance that provides a termination for a logic device transmission line to help reduce interconnect signal distortion (discussed separately above) |
| coupled - linked together (discussed separately above) | coupled - directly connected (discussed separately above) |
| pins - a conductor configured to make an electrical connection (discussed separately above) | pins - A small diameter metal rod used as an electrical terminal external to the semiconductor package housing (discussed separately above) |
| semiconductor package - package, such as an enclosure, for a semiconductor device (agreed upon construction); | semiconductor package - package, such as an enclosure, for a semiconductor device (agreed upon construction); |
| programmable termination - an electrical circuit that can be configured to provide various levels or degrees for the dissipation or absorption of electrical energy (discussed separately above) | programmable termination - The capability to configure the circuit to receive data signals from one of several available logic families (discussed separately above) |

There is nothing further for the Court to construe here. ON Semiconductor has separately addressed the proper construction for each of the terms "load elements," "coupled," "pins," and "programmable termination." These constructions, along with the parties' agreement as to the term "semiconductor package," leaves nothing more to construe. With an understanding of these individual terms, the larger phrase is readily understood.

Samsung, however, contends that more construction is needed only to get another chance to improperly read in limitations from the dependent claims (see, e.g., claim 14) or the specification relating to logic families. [*See*, *e.g.*, Ex. 6, Col. 1:64-2:2, 2:20-33, 6:44-48 (claim 14).] *See also, Phillips*, 415 F.3d at 1323. For the same reason as stated above, this attempt should be rejected.

III. U.S. PATENT NO. 5,563,594

A. Introduction

Asserted claim 8 recites:

> 8. A data conversion circuit, comprising:
> ***a register having an input coupled for receiving parallel input data and having an output***;
> ***a multiplexer having an input coupled to said output of said register for providing serial data***;
> a ***comparator*** having first and second inputs and an output, said first input receiving a first ***control signal***, said second input receiving a second ***control signal***, said output providing a compare signal having a first state when said ***first and second control signals match***; and
> a down counter responsive to said compare signal for initializing a count value and responsive to a ***clock signal*** for counting down to generate a ***transfer data signal*** having a symmetric duty cycle to enable transfer of said parallel input data to said ***register***.

The ’594 patent generally addresses the problem of passing various channels of information through a narrower stream. This problem is similar to having various lanes of commuter traffic converge into a one-lane tunnel. Leaving this problem to the drivers to resolve can lead to a chaotic situation. If, however, an appropriate configuration of traffic signals were implemented that sequentially allowed cars from the different lanes to enter and pass through the tunnel in an orderly manner, the situation is dramatically improved.

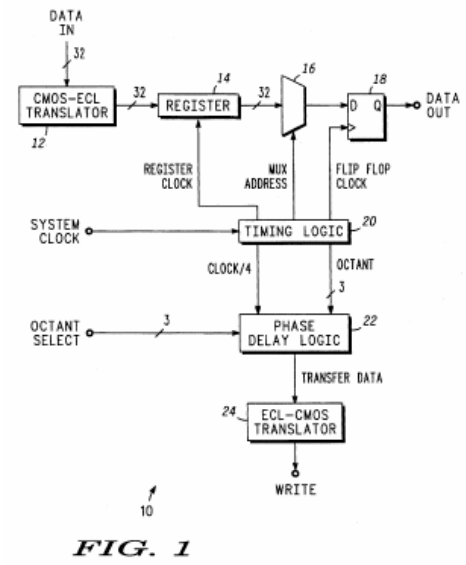

FIG. 1

In the context of the '594 patent as shown in Figure 1, the "tunnel" is the DATA OUT line and the multiple lanes of cars are the multiple lines of DATA IN (shown as 32 lines). [*See* Ex. 14, Col. 2:9-20.] Moreover, multiplexer 16 is important to funnel the multiple lines of information onto DATA OUT. [Ex. 14, Col. 2:15-18.] Multiplexer 16 along with the other circuitry (e.g, REGISTER 14, TIMING LOGIC 20, PHASE DELAY LOGIC 22, AND TRANSLATOR 24) are, therefore, analogous to a configuration of traffic signals that provides for an orderly flow of traffic through the tunnel. [*See* Ex. 14, Col. 2:7-3:29.]

In a different embodiment described in Figure 3, the '594 patent describes the reciprocal situation of distributing one input line to various output lines. [Ex. 14, Col. 5:31-6:12.] This is analogous to a tunnel opening up to various lanes of traffic.

B. The Disputed Claim Construction Issues

1. "Coupled"

| **ON Semiconductor** | **Samsung** |
|---|---|
| linked together | *The meaning of this term requires no construction. To the extent a construction is necessary, the term should be construed as:*<br><br>directly connected (from '644 patent) |

This term also appears in the '644 patent, discussed above. A proper analysis here, however, demonstrates that the same construction is applicable. The coupling of circuit components can occur in several ways; it can be achieved by capacitive or inductive coupling or it can be achieved by a direct connection to name a few examples. See discussion supra part IV B 4. The claims do not exclude that a "coupling" can be by other than direct connection. For example, the recitation in asserted claim 8 of "a register having an input coupled for receiving parallel input data" does not preclude capacitive or inductive coupling; nor does any other

aspect of claim 8 exclude capacitive or inductive coupling. Similarly, claim 8's recitation of "a multiplexer having an input coupled to said output of said register" does not exclude that this coupling can be capacitive or inductive coupling.

Although the specification describes certain direct connections that it characterizes as couplings, it nowhere indicates that the invention excludes other couplings or re-defines this well-understood term. [*See, e.g.*, Ex. 14, Col. 3:38-64.] Instead, the inventors only sought to provide examples that could be extended to broader concepts [*See, e.g., Id.*, Col. 6:29-37.]

Extrinsic evidence further confirms that the ordinary meaning of "coupling" includes "[a] mutual relation between two circuits that permits energy transfer from one to the other." [Ex. 15 at119.] This reference further clarifies that "[c]oupling may be direct through a wire, resistive through 'a resistor, inductive through a transformer or choke, or capacitive through a capacitor." [*Id*.] It also demonstrates, consistent with the intrinsic evidence that Samsung's construction is too narrow because a "coupling may be a direct wire" (i.e., a "direct connection") but can include more including capacitive or inductive couplings. [*Id*.]

2. "A Register Having an Input Coupled for Receiving Parallel Input Data and Having an Output"

| **ON Semiconductor** | **Samsung** |
|---|---|
| *It is ON Semiconductor's position that the Court need not construe this entire phrase. Instead, ON Semiconductor believes that the phrase can be understood according to the plain and ordinary meaning of its constituent terms or words.*<br><br>*If the Court is inclined to construe this phrase, ON Semiconductor contends that it can be understood simply by construing the following terms:*<br><br>register - a device capable of retaining or storing information.<br><br>coupled - linked together (discussed separately above) | A storage circuit that receives each bit of the input data simultaneously over several input lines<br><br>*Samsung further proposes the following constructions:*<br><br>coupled – linked together (discussed separately above) |

Here, the inventors claimed their invention using common terms familiar to those of ordinary skill in the art. Once again, Samsung seeks to construe a phrase that is clear on its face so as to rewrite it. If this phrase needs any clarification, however, it can be achieved by construing its constituent terms, in particular, "register" and "coupled." Having separately addressed "coupled," all that is left is to construe "register."

A register is an extremely well-known device to those of ordinary skill in the art. The inventors of the '594 used the term "register" consistently as a device capable of retaining or storing information. For example, the specification recites that "the input data is translated (12) and ***stored in a register*** (14)." [Ex. 14. at Abstract.] Moreover, the specification's recitation of "a data register is typically embedded within an integrated circuit that ***periodically receives new data*** sourced by external logic, or sources new data for external logic" indicates that from time to time a register may receive and store new information and make it available for other operations. [Ex. 14, Col. 1:14-17.] The specification extensively describes a preferred embodiment that involves many details of registers, but does not limit the claim to that embodiment, and in no way uses the term in any way contrary to its plain and ordinary meaning. [*See*, *e.g.*, Ex. 14, Col. 1:8-31.] Acumed, 483 at 808 (rejecting construction limited to characteristics of the patent's single preferred embodiment, finding a "preferred embodiment cannot be the only product covered by the claims; if it were, the claims themselves would be unnecessary").

Indeed, even Samsung's tortured construction of the larger phrase acknowledges that a register is a storage circuit: "A ***storage circuit*** that . . ." Because Samsung seemingly has no dispute with ON Semiconductor's construction of "register," it should be adopted by the Court.

With proper constructions for both "register" and "coupled," the larger disputed phrase is readily understood. A dispute only arises out of Samsung's attempt to rewrite the larger phrase, which should be rejected by the Court.

In attempting to add new limitations, Samsung improperly equates "coupled for receiving" with "receives." "Coupled for receiving" simply means that the circuit is connected and is able to receive a signal. "Receives" means that the signal is active and it is being received. There is a significant difference in the two definitions. The headlights of a car are "coupled to receive" electrical power whether they are on or off, but they only "receive" electrical power when they are turned on. The same distinction applies here.

Also, Samsung attempts to narrow the clear phrase "parallel input data" into "each bit of the input data simultaneously over several input lines." The plain meaning of the term does not require these very specific details. The only way Samsung arrives at its proposed construction is to read in limitations from the specification or to create the limitations itself from whole cloth which should be rejected. *See Phillips*, 415 F.3d at 1323.

Finally, Samsung is not even complete in its effort to rewrite the claim. Samsung does not address the portion of the disputed phrase that recites "and having an output." The tenets of claim construction make clear that every word of a claim must be given meaning, which Samsung does not do. *See, e.g., In re Gabapentin Patent Litig*., 503 F.3d 1254,1263 (Fed. Cir. 2007) (holding "construction adopted by the district court gives full meaning to every word of the entire claim term"); *Bicon, Inc. v. Straumann Co*., 441 F.3d 945, 950 (Fed. Cir. 2006) ("[C]laims are interpreted with an eye toward giving effect to all terms in the claim.").

3. "A Multiplexer Having an Input Coupled to Said Output of Said Register for Providing Serial Data"

| **ON Semiconductor** | **Samsung** |
|---|---|
| *The Court need not construe this, however, if* | A circuit that sequentially transmits the |

| | |
|---|---|
| *the Court is inclined to construe this, ON Semiconductor contends that the phrase can be understood with the following construction:*<br><br>Multiplexer - a device capable of manipulating multiple streams of digital information<br><br>coupled - linked together (discussed separately above)<br><br>Register - a device capable of retaining or storing information (discussed separately above) | parallel input data from the register one bit at a time over a single output line<br><br>*Samsung further proposes the following constructions:*<br><br>coupled – linked together (discussed separately above) |

With the discussion of the terms "coupled" and "register" above, the Court need only further construe the term "multiplexer." The claims of the '594 patent describe two forms of multiplexers –one that receives serial data and outputs parallel data (see claim 14) and another that receives parallel data and outputs serial data (see claim 8). The specification of the '594 patent also describes both of these kinds of multiplexers. [*See* Ex. 14, Abstract, FIG. 1, (parallel to serial), FIG. 3 (serial to parallel), Col. 2:-7-3:30, 5:31-6:12.] The multiplexer described in the '594 patent is able to convert parallel data to serial or serial data to parallel, or generally speaking, manipulate multiple streams of digital information. ON Semiconductor's proposed construction covers both types of multiplexers.

The extrinsic evidence is consistent with ON Semiconductor's construction in noting that "Multiplexing means transmitting a large number of information units over a smaller number of channels or lines." [*See*, Ex. 16 at 175-182.] Essentially, this describes a parallel to serial multiplexer. The Modern Dictionary of Electronics acknowledges that a multiplexer can also function in reverse, which is a serial to parallel multiplexer. [Ex. 3 at 648-649.]

Samsung, by contrast, improperly limits a multiplexer to only the parallel-to-serial variety. This limitation should be rejected as contrary to the intrinsic and extrinsic evidence.

4. "Comparator"

| **ON Semiconductor** | **Samsung** |
|---|---|

| | |
|---|---|
| an electronic device that receives input from two or more sources and provides an output responsive to a comparison of the inputs | A device whose output signal depends on the result of comparing two data items |

ON Semiconductor's construction encompasses the full scope of the term and is fully consistent with the claims, the specification, and the extrinsic evidence. As its name implies, a comparator is a circuit that compares two or more inputs. For example, the comparator described in the specification of the '594 patent is actually a six-input comparator that receives input from six digital signals. The specification describes that "[w]hen the 3-bit OCTANT signal matches the externally-supplied 3-bit OCTANT SELECT signal, the COMPARE signal is asserted as logic one" (i.e., a total of six bits). [Ex. 14, Col. 4:1-4.] Moreover, extrinsic evidence demonstrates the role of multi-input comparators.

For example, U.S. Patent 6,157,221 discloses a three-input comparator. Other references similarly discuss three- and four-input comparators. [*See, e.g.*, Ex. 18 at 1-4; Ex. 19 at 210-14; Ex. 20 at 565-73; Ex. 21 at 1-2; Ex. 22 at 135; Ex. 23 at 304-21; Ex. 24 at 111-114.]

Contrasting, Samsung seeks to improperly limit this term to two inputs. While some comparators may have two inputs, others have more, including the comparator of the '594 patent. There is no reason to limit the number of input lines, to two, three, or four. ON Semiconductor's construction captures this aspect of the term and should therefore be adopted by the Court.

5. Signal Terms – "Control Signal," "Clock Signal," and "Transfer Data Signal"

Samsung disputes the meaning of three terms involving the word "signal" ("control signal," "clock signal," and "transfer data signal") but does not appear to dispute the term "signal." Thus, to reduce the issues for the Court, ON Semiconductor also incorporates the term "signal" in its constructions. The parties' disputes, therefore, come down to the meaning of the terms "control," "clock," and "transfer data" and how they may modify the word signal. None of

these terms is extraordinary, and they need little, if any, construction by the Court. Samsung once again simply seeks to rewrite these otherwise straightforward terms.

a. "Control Signal"

| ON Semiconductor | Samsung |
|---|---|
| a signal that conveys information about regulation or guidance | A signal for controlling the phase of the transfer data signal |

The term "control signal" also appears in the '001 patent, discussed above. A proper analysis here, however, demonstrates that the same construction is applicable. Samsung, however, deviates from the tenets of claim construction to arrive at improper constructions both times.

Asserted claim 8 of the '594 patent describes that the claimed "control signals" are input to the claimed "comparator." In this way, the "control signals" serve to control the output of the comparator. The specification describes a "WRITE control signal" that serves to control the manner in which certain data is to be written to certain circuitry. In this example, the control signal conveys information about the regulation or guidance of other circuitry.

Reference to extrinsic evidence also supports ON Semiconductor's more general construction. For example, Merriam-Webster's Collegiate Dictionary defines "control" as "to exercise restraining or directing influence over: regulate." [Ex. 2, p. 252.] Similarly, IEEE Standard Dictionary of Electrical and Electronics Terms defines it as "[b]roadly, the methods and means of governing the performance of any electric apparatus, machine, or system." [Ex. 34, p. 133.] *See Phillips*, 415 at 1318 (discussing usefulness of technical dictionaries).

In contrast, Samsung improperly seeks to import limitations, apparently from a passage of the specification that discusses "controlling the phase of a data transfer signal to set the proper timing for reading or writing to a data register." [Ex. 14, Col. 1:6-9.] But claim 8 does not recite anything about "the phase" of the transfer data signal; and in any event, there is no basis to

import this limitation into claim 8. *See Phillips*, 415 F.3d at 1323; *Acumed*, 483 F.3d at 808 (adhering to the adage that "limitations from the specification are not to be read into the claims") (internal citations omitted).

b. "Clock Signal"

| **ON Semiconductor** | **Samsung** |
|---|---|
| a signal that conveys clocking or timing information | A signal consisting of a series of pulses used for synchronizing the data conversion circuit |

The issue here is how the term "clock" modifies signal. "Clock" is an extremely well understood term in the art to which it pertains. A review of the claims reveals that a clock is generally used in various electronic circuits to convey timing information, consistent with ON Semiconductor's construction. For example, the recitation in claim 8 of "a clock signal for counting down" can be understood as providing a signal with timing information for counting down. Moreover, the recitation in claim 9 of "said ***clock input*** being coupled for receiving said clock signal" similarly relates to a signal with timing information. The specification is similarly consistent in describing that "***[t]iming logic*** 20 operates in response to a SYSTEM ***CLOCK signal***, running for example at ***2.5 gigahertz***." [Ex. 14, Col. 2:21-24.] The specification further highlights the timing aspects of a clock signal when it explains that "[t]he internal ***timing*** generation logic asserts a ***clock signal*** to load the data register." [*Id.*, Col. 1:40-41.]

Samsung again attempts to rewrite an otherwise straightforward term. Here, Samsung attempts to limit a clock signal to "a series of pulses" that in turn raises the issue of what a "pulse" is since it is nowhere mentioned in the specification. Nor does the asserted claim include anything about "synchronizing the data conversion circuit." In fact, no claim in this patent includes this limitation. Even the specification is silent on this point. The only variant of the word "synchronizing" found in the specification is a discussion of "flipflops 48, 56, and 60

operate as a 3-bit ***synchronous*** down counter." [*Id.*, Col. 4:6-9.] There is nothing about this passage that justifies importing it into a construction for the very simple term "clock signal."

c. "Transfer Data Signal"

| **ON Semiconductor** | **Samsung** |
|---|---|
| a signal that conveys information regarding the transfer of data | A periodic signal requesting that external logic write the next set of parallel input data to the register |

The plain meaning of this phrase is understood as a signal relating to the transfer of data. Just as "control signal" and "clock signal" are easily understood terms, so is "transfer data signal." Asserted claim 8 clearly recites "a transfer data signal having a symmetric duty cycle to enable transfer of said parallel input data to said register." The plain meaning of this phrase is that the "transfer data signal" relates to the "transfer of . . . data." There is nothing ambiguous here. The specification is similarly clear in describing that "OCTANT SELECT signal '001 sets the proper phase delay before asserting TRANSFER DATA to the external logic to send the next DATA IN word." [*Id.*, Col. 4:16-21.] As described here, the TRANSFER DATA conveys information about when the piece of data called "DATA IN word" is to be transferred.

Samsung improperly attempts to import an "external logic" limitation from the specification. [*See, e.g.*, *id.*, Col. 2:62-67.] Samsung also attempts to include a limitation that the "transfer data signal" should be periodic and serve to request a write command, none of which is proper. *See Phillips*, 415 F.3d at 1323.

6. "First and Second Control Signals Match"

| **ON Semiconductor** | **Samsung** |
|---|---|
| *The Court need not construe this, however, if the Court is inclined to construe this, ON Semiconductor contends that the phrase can be understood with the following constructions:*<br><br>***control signals:*** an electrical effect that conveys information about regulation or guidance (separately construed above); | The data represented by the first and second control signals is the same |

| | |
|---|---|
| ***match:*** corresponding, suitably associated, or harmonious | |

Having separately construed "control signals," the only real dispute here is as to the meaning of "match." This is not a complex term, indeed, it is not even a technical term. One of ordinary skill in the art, indeed one familiar with the English language, understands the term "match." For example, a left shoe may match a right shoe. They are not the same shoe, having certain opposite qualities, but they are nonetheless suitably associated or harmonious with one corresponding to the other. Likewise signals with corresponding or harmonious qualities may be said to match. For example, two signals with the same frequency but with different amplitudes may be said to match (e.g., frequency modulation). In a different application, however, signals with different frequencies but similar amplitudes may be said to match (e.g., peak detection). Still in other applications signals of approximately the same value may be said to match (e.g., a 115 volt household voltage matches a device rated for 120 volts).

In the context of the claims, the inventors, being at least of ordinary skill in the art, were free to use the word "same" or "equal." But they did not; they chose the word "match." Accordingly, they should be afforded the full breadth of their word choice. *See, e.g., Rexnord Corp. v. Laitram Corp.*, 274 F.3d 1336, 1342 (Fed. Cir. 2001) ("[U]nless compelled to do otherwise, a court will give a claim term the full range of its ordinary meaning as understood by an artisan of ordinary skill."); *In re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir. 2000) ("[C]laims are given their broadest reasonable interpretation consistent with the specification."). In the context of asserted claim 8, there is nothing to suggest that where the "first and second control signals match" they must be the same. In fact, because the claim is referring to a comparator, the signals may "match" when the magnitude of one exceeds the magnitude of the other such as discussed in a reference cited by Samsung itself. [*See* Ex. 25, pp. 479 ("comparator circuit . . . a circuit whose output indicates whether one of its two inputs higher than, equal to, or lower than the

other input").] Samsung's own reference clarifies that matching items need not be the same. [*Id.*, p. 1323 ("match . . . to check for identity ***or similarity***").]

Extrinsic evidence, consistent with the intrinsic record, also supports ON Semiconductor's construction. For example, Merriam-Webster's Collegiate Dictionary, 714-715 (10th ed. 2001) defines "match" as "a person or thing equal or similar to another," "a pair suitably associated," "to be the counterpart of," "to compare favorably with," "to harmonize with," or "to provide with a counterpart." [Ex. 2 at 714-15.]

Not surprisingly, Samsung's proposed construction seeks to drastically narrow the breadth of the claim term "match" to only mean "the same." As the definitions quoted above show, equality is one type of "match," but not the only type, and there is no proper reason to limit such a simple word to the most restrictive possible interpretation.

## IV. U.S. PATENT NO. 5,000,827

### A. Introduction to the Claims

The '827 patent is titled "Method and Apparatus for Adjusting Plating Solution Flow Characteristics at Substrate Cathode Periphery to Minimize Edge Effect." The claim terms in dispute are recited in claim 1:

> 1. A method of forming ***metallized bumps*** on predetermined terminal areas of a planar substrate, ***said bumps being of substantially uniform height across said substrate***, wherein said method comprises:
> (a) providing a planar substrate having thereon a multiplicity of terminal areas;
> (b) applying an electrical potential having a first electrical polarity to said terminal areas;
> (c) applying an electrical potential having a second electrical polarity to an electrical terminal immersed in a container of an electroplating solution;
> (d) exposing said substrate to said electroplating solution to permit the growtth of said metallization ***bumps*** on said terminal areas;
> (e) controlling the growth of said metallization ***bumps*** in a predetermined region of said substrate by altering the metallic ion concentration of said electroplating solution in said predetermined region;
> (f) providing said container with an opening whose shape approximates that of said substrate;

(g) positioning said substrate proximate to said container opening;
(h) providing an inlet within said container for pumping said solution into said container, said solution exiting said container through said opening;
wherein said metallic ion concentration of said electroplating solution is changed by:
(i) in step (f) altering the size of said opening;
(j) in step (g) altering the distance of said substrate from said container opening; and
(k) in step (h) ***altering the flow rate of said solution through said opening***.

[Ex. 26, Col. 6:30-62.]

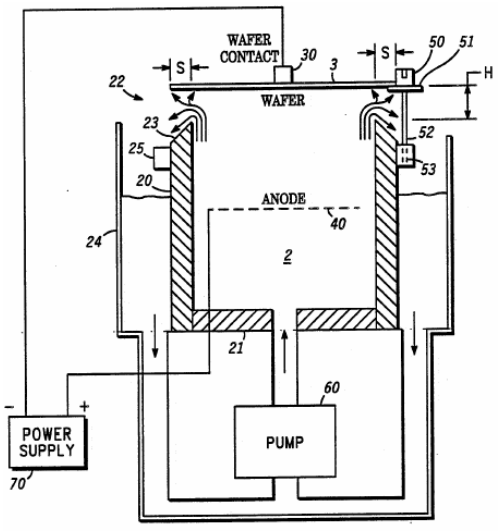


FIG. 7

The '827 patent is generally directed to building up metal structures, called bumps, on a surface of a wafer, called a substrate, using electroplating utilizing a cup having an opening over which a wafer is placed. [Ex. 26, Fig. 7.] Outside the context of this patent, electroplating is most commonly used to place a thin layer of a precious metal such as gold or silver on an article made from a less expensive metal. The '827 Patent teaches using electroplating layers of metal in selected areas of a chip, not the entire surface, to buildup uniform "bumps" of metal over the device. The claims of the '827 patent are directed to a method for electroplating semiconductor chips by forming uniform height metallization bumps across a substrate.[10]

To realize uniform height metallization bumps, the '827 patent solves the problem of the "edge effect" which causes some of the bumps to grow higher than others by reducing the

[10] In electroplating, an electric field is generated in a solution of ions to plate certain areas with metal ions, such as terminal areas of electrical circuits that are formed on the wafer. [*See generally*, Ex. 27, pp. 94-103.] To allow for plating of the wafer, an anode and a cathode of the circuit is immersed in a solution that contains metal ions. [*Id*.] A DC voltage is provided to the anode and cathode. [*Id*. at 96-98.] The metallic ions carry a positive charge and are attracted to the wafer that has a negative charge. [*Id*.] When the ions reach the wafer, the negative charge on the wafer provides electrons to reduce the positively charged ions to a metal on the wafer. [*Id*.] Through this electro deposition process, metal layers can be deposited on the wafer. [*Id*.]

metallic ion concentration near edge of a circular wafer, typically made of silicon and usually 8 or 12 inches in diameter. The patent teaches that because of the greater electric field intensity near the edge, more material may be deposited there resulting in greater bump height at the edge than in the interior portions of the wafer. [*See, e.g., id*., Col. 2:29-43; *see also* Ex. 27, p. 116 (illustrating the edge effect in Fig. 4.24).]

The '827 patent discloses three parameters that may be optimized to offset the edge effect and create uniform height metallization bumps across a substrate. [*See, e.g.*, Ex. 26, Col. 2:63-3:13, 6:58-62.] A first parameter is the distance of the wafer from the container opening. [*Id*., Col. 2:67-3:1, 5:31-42, 6:59-60.] A second is the size of the opening relative to the wafer size. *[Id*., Col. 2:66-67, 5:18-30, 6:58.] A third is the flow rate of the solution through the container opening. [*Id*., Col. 3:1-3, 6:61-62.]

B. The Disputed Claim Construction Issues

1. "Said Bumps Being of Substantially Uniform Height Across Said Substrate"

The first dispute is whether the preamble phrase "said bumps being of substantially uniform height across said substrate" limits claim 1, and, if it does, its proper construction.

a. The Preamble Phrase Merely Recites the Purpose for the Invention, and Is Not a Limitation.

This phrase requires no construction as it merely recites the purpose or anticipated result of the invention and is not a claim limitation.[11] The stated purpose of the claim preamble is the same purpose stated in the specification, and the complete invention that is recited in the claim

[11] ON Semiconductor agrees that "metallization bumps" limits claim 1 because it is also recited in the body of the claim. That fact does not warrant treating the preamble as a limitation, however, because the term is also found in the body of the claim. Thus it is not necessary to construe the preamble to provide the complete structure of the claim**.**

body. [*See, e.g., id.*, Col. 3:9-13, 6:30-62.] In the Summary of the Invention section, the patent expressly states that it is "an ***object*** of the present invention to provide an electroplating method . . . which produce metallized bumps of substantially uniform height across a substrate including the edge(s) thereof." [*Id.*] Other parts of the patent also reiterate this same purpose. [*See id.*, Col. 1:9-13 (the field of application for the invention is for the "***formation of uniform-thickness metallization bumps*** on terminal areas of electrical circuits on a substantially planar substrate, particularly near the edge thereof"); 1:15-17 (describing that the invention has "***utility in the plating of metallization bumps*** on predetermined areas of silicon wafers . . . .").]

All of the steps for achieving this purpose, including the essential steps (i), (j), and (k) for realizing uniform height metallization bumps, are recited in the claim body. In other words, the preamble phrase is immaterial for the practice of the invention, and is not a limitation. *See Intirtool, Ltd. v. Texar Corp.*, 369 F.3d 1289, 1295 (Fed. Cir. 2004).

b. If the Court Finds that the Preamble is a Limitation, It Should Adopt ON Semiconductor's Proposed Construction.

Alternatively, if the Court finds that the preamble acts to limit claim 1, then the Court should adopt ON Semiconductor's proposed construction for this phrase.

| **ON Semiconductor** | **Samsung** |
|---|---|
| approximately the same distance between the top of the bump and the top surface of the substrate | small mounds of metal utilized as contacts having substantially the same height above the semiconductor pad on which they are formed across the wafer |

ON Semiconductor's construction flows directly from the ordinary meaning, consistent with the description provided in the specification The claim requires that the bumps have "substantially uniform height across said substrate." The ordinary meaning of "substantially uniform" is "approximately the same." [*See, e.g.*, Ex. 30, p. 1321 (uniform: "always the same; unvarying," "without fluctuation or variation; consistent," or "being the same as another or

others; identical.").] And, as to the term "height," the patent describes that, by using the claimed process, bump height variation of 8 microns, and even about 4 microns, across the wafer was achieved. [Ex. 26, Col. 5:55-58, 5:64-6:1, FIGS. 9-10; *see also* Ex. 26, Col. 5:40-42 (disclosing result of one embodiment of the invention as "edge bumps which are nearly identical in height to bumps elsewhere across the wafer diameter").] This description makes it clear that (i) the bumps are not identical because there remains a 4 to 8 micron difference in their heights, and (ii), the term "height" should refer to the distance between a common reference point, such as the top surface of the substrate, and the highest point on the bumps that are formed on the substrate.

Samsung's construction, which attempts to limit metallization bumps to those formed on "semiconductor pads," is flawed because: (1) there is no requirement that the metallization bumps be formed only on a "pad;" and (2) the proposed limitation that the bumps are formed on top of a "semiconductor" is directly contradicted by the '827 patent specification.

That lack of support for Samsung's proposed limitation that the bumps be formed on a "pad . . . across the wafer" is clear from reference to other limitations recited in the claim and the specification. For example, the claim requires that the metallization bumps are formed on "terminal areas" of a substrate. [*See* Ex. 26, Col. 6:30-31, 6:41-43.] In the context of the patent, a terminal area refers to the region that is in the vicinity of a terminal[12] of a semiconductor device. For instance, the patent describes that "a hole or window 18 has been etched through the oxide 38 down to a terminal area (not shown) of the underlying substrate" where, for example, a diode is formed. [Ex. 26, Col. 1:33-37; 1:40-42.] In this instance, the patent refers to the area beneath the oxide in the vicinity of a terminal of a semiconductor device as a terminal area. In

[12] A terminal is the point of connection to an electronic device. [*See, e.g.*, Ex. 34, p. 710 ("An externally available point of connection to one or more electrodes or elements within the device.").]

other instances, the terminal area is described as on top of the top layer 19, which is also in the vicinity of a terminal of a semiconductor device that is formed underneath. [*See id*., Col. 1:50-52 ("over the top metal ***region*** 19."); Col. 1:66-67 ("onto predetermined terminal areas of a silicon wafer, such as terminal ***area*** 19 . . . ."). ] The patent uses the phrase terminal "area" in the ordinary sense, i.e., in the vicinity or a region, where a terminal exists. [*See* Ex. 30, p. 126 (area: "a section or region, as of land . . .").] But Samsung's construction would require that "terminal area" be a specific structure because it would require that "area" be equated with "pad." This is not the ordinary meaning and the specification shows that a terminal "area" refers to a "region" or "vicinity" around the terminal, consistent with the ordinary meaning.

Second, the requirement that the bump be formed on a "semiconductor" material is in direct contravention of the specification which explains the bumps are formed on top of a metal layer. With reference to Figure 3B, the patent describes that "the window 18 of Fig. 3A has been filled with top metal 19" and that the bump is formed on this top metal 19. [Ex. 26, Col. 1:43-44.] Samsung's proposal is therefore contrary to the specification.

2. "Metallization Bumps"

| **ON Semiconductor** | **Samsung** |
|---|---|
| "the accumulation of a metal layer or layers" | "small mounds formed of metal on a semiconductor pad that are utilized as contacts." |

The intrinsic evidence makes clear that metallization bumps are a "non-planar accumulation of a metal layer or layers" on a substrate. Samsung's proposal is flawed because it improperly limits the claim to the preferred embodiment and excludes the preferred embodiment.

The patent specification and prosecution history show that a metallization bump is formed from the deposition of metal layer or layers. First, the patent describes that multiple layers are deposited to form the metallization bump. [*See* Ex. 26, Col. 5:46-49 ("The invention described herein was used successfully to plate bumps comprising an initial tin layer of silver

and a subsequent layer of tin, resulting in metallization bumps as depicted in FIG. 3C.").] Second, the prosecution history shows that both the examiner and applicants understood that deposition of metal layers disclosed metallization bumps. For instance, the examiner rejected the claims based on JP '797 and JP '039 references that disclosed depositing a metallic film or layer on a semiconductor substrate. [*See* Ex. 39, p. 3; Ex. 31 at Translation p. 1, Sec. 3; Ex. 29 at Translation p. 1, Sec. 3.] When faced with the examiner's rejections, the applicants did not dispute that the references disclosed metallization bumps, but distinguished them based on the prior art's failure to disclose other elements of the invention. [Ex. 28, pp. 3-4.] With regard to the JP '797 reference, the applicant acknowledged that this reference "discloses electroplating apparatus somewhat similar to that used by applicants," but noted that the difference between its claim and this reference was that the JP '797 reference did not teach to "chang[e] the ion concentration by the three altering steps disclosed and claimed by applicants . . . ." [*Id.*]

The proper construction should also makeS clear that the accumulation be "non-planar." The patent distinguishes between the metal layers that form the metallization bump and the metal layers that are deposited in the terminal region 19 to form the top metal. As shown in Fig. 3B, the metal layers that fill the hole 18 results in a flat layer of top metal on the substrate. [Ex. 26 at FIG. 3B, Col. 1:43-49.] Then, as shown in Figure 3C, the metallization bump is formed on the flat top metal. [*Id*. at FIG. 3C, Col. 1:50-52.] The construction should, therefore, distinguish the "planar" accumulation of a metal layer to form the top metal and the "non-planar" accumulation of a metal layer to form the metallization bump. This also recognizes the mound shape bump in Fig. 3C, including that the "bump" should not be limited to just this particular shape, and that other accumulations in different shapes can qualify as a bump. [*Id.*] Indeed, the patent makes clear that it should be understood by "practitioners in the art that the present invention has broad

utility in many metallization bump processing applications and is not intended to be limited to implementations such as that shown in Figure 3 and 4." [*Id*., Col. 1:56-60.]

Samsung's construction appears to be based heavily on extrinsic sources such as dictionary definitions that contradict the intrinsic record. In the Joint Claim Construction Statement [D.I. 117 at Exs. pp. 2-7], Samsung refers to various dictionaries that define a "bump" as "a small mound."[13] Samsung then incorporates this definition into its construction almost verbatim. [*Id.* at 2.] This flawed approach has led Samsung to propose a construction that is limited to the preferred shape of the bump, but that also excludes a preferred use of the metallization bump.

Samsung's apparent resort to dictionary definitions to reach a construction that is limited to the preferred shape of a mound as disclosed in Fig. 3C is improper. *See Phillips,* 415 F.3d at 1323. Indeed, Samsung's construction is all the more incorrect because it is contrary to the patent's admonition that the invention is not limited to the mound shaped implementation shown in Fig. 3.[14] [*See* Ex. 26, Col. 1:56-60.]

3. "Altering the Flow Rate of Said Solution Through Said Opening"

| **On Semiconductor** | **Samsung** | **Agreed Construction** |
|---|---|---|
| changing the volume of electroplating solution flowing per unit of time flowing out of the opening | changing the volume of electroplating solution per unit of time through the opening of the solution container during the formation of the metallic bumps to control their growth in a predetermined region of the | flow rate: "volume flowing per unit of time " |

[13] [*See, e.g.*, Ex. 33, pp. 16 ("Bump. A small mound or hump that is formed on the chip or the substrate bonding pad and is used as a contact in facedown bonding."); Ex. 3, p. 121 ("bump-- . . . A small mound is formed on the device (or substrate) pads, and is utilized as a contact for face-down bonding.").]

[14] The inclusion of "small" in Samsung's construction renders the construction impermissibly vague, and should not be a part of any construction.

| | | |
|---|---|---|
| | substrate." | |

The parties agree on the meaning of "flow rate" that is recited in the disputed phrase, and ON Semiconductor's construction substantially overlaps with Samsung's construction. ON Semiconductor objects, however, to Samsung's addition of "during the formation of the metallic bumps to control their growth in a predetermined region of the substrate" as part of its construction. There simply is no need to include this extraneous language because it would only result in confusion and render other claim limitations superfluous.

The claim term simply requires adjusting the flow rate of the solution through the container opening. Although the invention adjusts the flow rate to adjust ion concentration to control the growth of metallization layers, these requirements are not expressly recited in the claim term at issue, and are in fact recited elsewhere in the claim. For instance, claim 1 recites "(e) controlling the growth of said metallization bumps in a predetermined region of said substrate by altering the metallic ion concentration of said electroplating solution in said predetermined region;" wherein the "(h) . . . metallic ion concentration . . . is changed by" the step of "(k) . . . altering the flow rate of said solution through said opening." [Ex. 26, Col. 6:44-62.] Samsung's construction that includes the requirement of "during the formation of the metallic bumps to control their growth in a predetermined region of the substrate" seeks to incorporate step (e) into step (k). Samsung's approach is unnecessary, potentially confusing to a jury, and would render other limitations of the claim superfluous.

## V. U.S. PATENT NO. 5.252,177

### A. Introduction to the Claims

Samsung's '177 patent is titled "Method for Forming a Multilayer Wiring of a Semiconductor Device." Independent claim 8 is exemplary:

8. A method for forming an electrical connection on a semiconductor substrate between a ***first conductive layer*** and a second conductive layer through an intervening insulation layer formed over said ***first conductive layer***, said method comprising the steps of:

forming a ***photoresist pattern*** on said insulation layer;

after forming said ***photoresist pattern***, forming a contact hole by selectively etching out exposed regions of said insulation layer to ***expose a top surface of said first conductive layer***;

***removing remaining photoresist positioned on said insulation layer by plasma ashing to simultaneously form a protective oxide layer*** on said ***exposed top surface*** of said ***first conductive layer***; and

***removing said oxide layer before forming said second conductive layer on said exposed top surface of said first conductive layer***.

[Ex. 37, Col. 4:24-40.]

The ’177 patent is directed to methods for forming multilayer wiring. [*Id.*, Col. 2:19-20.] This is the microscopic wiring that interconnects the many transistors on an integrated circuit (also called a chip). In particular, the ’177 patent teaches a method for forming multilayer interconnects that maximize the contact area between two conductive layers to achieve a low contact resistance, and improve device performance. [*Id.*, Col. 3:22, 32-35.]

Figure 1A of the ’177 patent is helpful to understanding prior art techniques and the improvements the ’177 patent supposedly achieved. In the prior art, a conductive layer, such as aluminum is first deposited (11) and an insulating layer is deposited on top of the conductive layer (13). [*Id.*, Col. 1:24-29.] The next step is to create precisely spaced openings called “vias” that expose lower layer material through an opening in the upper layers, similar to a well exposing lower layers of soil by removing some of the upper layers in a small area. To do this, a protective photoresist is first applied over the insulating layer. [*See id.*, Col. 1: 31-33.] Two

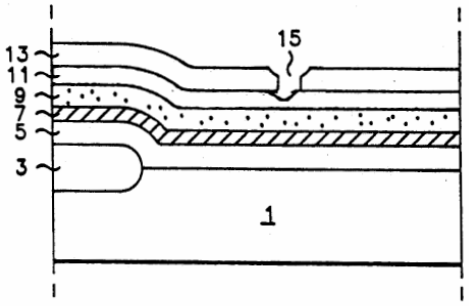


Fig. 1A
(Prior Art)

important qualities of the photoresist are that like photographic film, it reacts when exposed to light and it is an organic material that will react with oxygen.

The next step is to expose the photoresist layer to light using a predefined pattern that will expose those portions of the photoresist covering the insulating layer to light only where the via is to be formed and that will protect the rest of the insulating layer from exposure to light. This would be analogous to placing sheets of plywood or other material over the ground where a well is being dug and opening a hole in the plywood to expose where the well needs to go. A plasma etch process is then used to precisely remove portions of the exposed photresist and insulating layer to create each via in the insulating layer (essentially drilling the well) down to the underlying aluminum. [*See id.*, Col. 1:31-35.] Although the unexposed photoresist may be partially removed by the etch process, some of it still remains and must be removed. This is done through an oxygen plasma ash process. [*See id.*, Col. 1:50-63.] The use of oxygen is important because it reacts with the organic photoresist to effectively "burn it off" and create an ash. This would be like burning off the rest of the plywood after digging the well.

Importantly, the prior art also recognized that, during this ashing process, the oxygen in the plasma ash readily reacted with the now exposed aluminum to form an oxide layer. [*See, e.g.*, NN, Col. 5:9-13.] Thus after the ash is cleaned away, the oxide layer must also be removed, for example by an etching (sputtering) method that is similar to sand blasting that knocks the oxide layer off. [*Id.*] Everything described up to this point was known in the prior art; the named inventors of the '177 patent added nothing new here.

The alleged invention begins with the acknowledgement of the problem that the chemical and mechanical processes used to clear out the photoresit may damage the underlying wiring. [*See, e.g.*, Ex. 37, Col. 1:44-50.] Obviously this is undesirable. [*Id.*, Col. 1:67-2:2.] To protect

against this kind of damage, the specification describes taking advantage of the inherent natural tendency of the metal layer to oxidize in the presence of oxygen during the ashing step and to allow an oxide layer to form to a particular thickness under particular plasma ashing conditions. [*Id.*, Col. 2:61-3:8, Fig. 2A.] In other words, the claimed invention here is to take advantage of the serendipitous presence of the oxide layer formed by the ashing process.

B. The Disputed Claim Construction Issues

1. "Removing Said Photoresist Pattern Positioned on Said Insulation Layer by Plasma Etching Simultaneously Forming a Protective Oxide Layer" (claim 1) and

2. "removing Remaining Photoresist Positioned on Said Insulation Layer by Plasma Ashing to Simultaneously Form a Protective Oxide Layer" (claim 8)

These phrases are discussed together because they recite similar steps of removing the photoresist and simultaneously forming the protective oxide layer, the only difference being that the photoresist is removed by plasma *etching* in claim 1 and plasma *ashing* in claim 8.

| **ON Semiconductor** | **Samsung** |
|---|---|
| Claim 1: "getting rid of all the photoresist on the insulation layer by plasma etching and forming a protective oxide layer at the same time as removing the photoresist."<br><br>Claim 8: "getting rid of all the remaining photoresist by plasma ashing and forming a protective oxide layer at the same time as removing the photoresist." | The meaning of this phrase requires no construction. To the extent a construction is necessary, the phrase should be construed as "removing photoresist." |

Before discussing the construction for these larger phrases, the disputes related to their constituent parts will be addressed first.

a. "Removing Said Photoresist Pattern;" and "Removing Remaining Photoresist"

The dispute here is whether all of the photoresist is removed during the plasma ashing step. ON Semiconductor contends that it is and Samsung does not provide a construction. The intrinsic evidence supports removal of all of the photoresist.

First, claim 8 actually requires removal of "remaining photoresist." Thus, the claim language clearly indicates that plasma ashing removes all of the photoresist. Also, the specification describes and shows in the figures that all of the photoresist is removed. [*See, e.g.*, Ex. 37 at Figs. 2A-2B; Col. 2:45-46; Col. 3:8-13 ("removing all the remaining photoresist").] The specification describes that a plasma etch is performed to selectively etch the third insulation layer 13 which removes some of the photoresist. [*Id.*, Col. 1:31-33, 50-53.] Then, it describes that oxygen plasma ashing should be performed to remove the remaining photoresist. [*Id.*, Col. 2:61-3:2.] Nothing in the intrinsic evidence teaches removing only some of the photoresist.

b. "Plasma Etching" and "Plasma Ashing"[15]

| **ON Semiconductor** | **Samsung** |
|---|---|
| ***plasma etching:*** An etching process for selective removal, such as used for forming a contact hole, using a plasma of ionized gases in which the ions are accelerated toward the material desired to be removed.<br><br>***plasma ashing*:** A process for removing an organic material through oxidation, such as a photoresist in a plasma of oxygen | ***plasma etching:*** The meaning of this phrase requires no construction. To the extent a construction is necessary, the phrase should be construed as "a process of removing one or more materials using plasma."<br><br>***plasma ashing***: The meaning of this phrase requires no construction. To the extent a construction is necessary, the phrase should be construed as "a plasma etch designed to remove photoresist." |

ON Semiconductor's construction properly accounts for the different processes used for plasma etch and plasma ash. Samsung asserts that they should have the same construction.

The intrinsic evidence shows that the inventors used the terms plasma etching and plasma ashing to describe distinct processes. In describing plasma etching, the patent describes a selective etching process that can be used to form a contact hole 15 [Ex. 37, Col. 1:31-33], or in

[15] ON Semiconductor has also noticed the Court as to invalidity of claims 1 and 3 in the Joint Claim Construction Statement based on lack of written description with regard to claim 1, and for being indefinite with regard to claim 3. [D.I. 117 at Exs. pp. 31-42.] Upon the Court's ruling on claim construction, ON Semiconductor reserves the right to file a motion challenging validity of these claims.

another step, forming the overlying layer "by formation of a pattern and selective etching." [*Id.*, Col. 2:4-7]. As to plasma ashing, the patent describes that it is performed to remove the remaining photoresist on the insulation layer after the step of plasma etching to form the contact hole, and to simultaneously form an aluminum oxide layer. [*Id.*,, Col. 1:50-57, 2:26-33, 2:61-66.] It is clear from the description that these are distinct processes used for different purposes, and are not interchangeable.

The distinction is also confirmed in the prosecution history. Initially, the applicants filed their application with five claims directed to methods based on "plasma ashing." [*See* Ex. 49, pp. 7-10.] Then the applicants added claims 6-15 that also recited "plasma ashing" and stated that they added these claims to "alternatively define Applicants' invention" from that claimed in claims 1-5. [*Id.*] After the notice of allowance the applicants filed an amendment that changed claims 1 and 6 to "plasma etching" from "plasma ashing." [Ex. 50, pp. 2-3.] The other claims continued to recite "plasma ashing." [*Id.*] In making this change, the applicants asserted that they were correcting the claims for "inadvertent typographic errors." [*Id.*, p. 3.] The applicants, therefore, considered plasma etching and plasma ashing different enough to "alternatively define" their invention and to amend their claims to highlight the distinction even after the notice of allowance.

Both the patent and authorities on plasma processing show that plasma etching involves selective etching with ion bombardment. As discussed above, all of the instances of etching used in the patent describe selective etching. Indeed, this understanding of etching in the patent is confirmed by the Modern Dictionary of Electronics: "[t]he selective removal of unwanted material from a surface . . . ." [Ex. 3, pp. 352 ("etching"), 754 ("plasma," "plasma etching").] The same dictionary describes etching as a "process using either acids or a gas plasma to remove

unwanted material from the surface of a wafer." [*Id.; see also* Ex. 51 at 16-17 (noting that "[t]he second feature that makes plasma discharges so useful is their ability to generate ions and to accelerate the ions to energies of 50 - 1000 eV in the vicinity of the deposition or etching substrate," and that "[e]nergetic ions are useful for sputtering, as in the sputter deposition of metals . . . [and] can also play a synergistic role in the deposition or etching of thin films").]

Samsung's construction in contrast would equate plasma etching and plasma ashing. This is contrary to both the intrinsic and extrinsic evidence that clearly show that the two processes are *alternative* removal processes and are not the same just because both use a plasma.

Plasma ashing is not characterized by high impact ion bombardment as in plasma etching, but rather removal occurs more through a reaction with oxygen. The difference is analogous to sand blasting (etching) versus burning off (ashing) a protective layer. [*See* Ex. 47 at 352-55 ("The application of plasma oxidation to photoresist removal was first suggested in 1968 by Irving [2]. He showed that conventional photoresists could be removed at rates as high at 2000 A/min.").] Oxidation only occurs with organic materials. [*See* Ex. 42, p. 211 (stating that in plasma ashing, "an oxygen plasma reacts readily with the organic resist but leaves inorganic films (such as oxide, nitride, polysilicon or metal) mostly intact.") The patent describes that plasma ashing should be used when removing the organic photoresist, which also naturally forms the aluminum oxide layer at the same time. [Ex. 37, Col. 2:30-3:7.] Further, the claims require using an oxygen plasma because other parts of the claim require formation of an oxide layer that requires the presence of oxygen. [Ex. 37, claim 1.]

c. "Simultaneous Form" and "Simultaneous Forming"

| **ON Semiconductor** | **Samsung** |
|---|---|
| "form at the same time"/ "forming at the same time" | forming as part of the plasma ashing/etching also used to remove photoresist |

ON Semiconductor's construction adheres to the express requirements of the claim and the ordinary meaning of the word "simultaneously;" that is, two occurrences or events are happening at the same time or concurrently. [*See* Ex. 30 at 1142 ("simultaneous": as "happening, existing, or done at the same time.").] The claim expressly requires that plasma etching/ashing is used to form the aluminum oxide layer at the same time that it is used to remove the photoresist layer. Indeed, the specification describes that the protective oxide layer should be formed under precise plasma ashing conditions of 500 SCCM, 4-5 Torr and 250-350 C to form a 30 to 80 Angstrom thick oxide layer, which are the same conditions when the photoresist is being removed. [Ex. 37, Col. 2:61-3:2.]

The problem with Samsung's construction is that it attempts to cover oxidation process that occurs before the oxygen is turned into a plasma (i.e., before plasma ashing has even begun). In other words, Samsung's construction suggests that the formation of the protective layer can occur in preparatory steps and not at the same time and under the same conditions as plasma ashing. This is contrary to the claim and specification, and should be rejected.

d. "Protective Oxide Layer"

| **ON Semiconductor** | **Samsung** |
|---|---|
| An oxide layer of a predetermined thickness (*e.g.*, a thickness of 30 to 80 Å for an aluminum conductor) that is used to prevent damage to an underlying layer by preventing reaction between the wiring, an organic solvent and water in subsequent processing steps. | An oxide layer sufficient to prevent damage to an underlying layer. |

Although the parties agree that the claimed protective oxide layer is used to prevent damage to an underlying layer, ON Semiconductor's construction captures the true scope of what the applicants allegedly invented. *See, e.g., Phillips*, 415 F.3d at 1322. Samsung, on the other

hand, proposes a construction that is overly broad and is not limited to the actual invention; indeed, it is so broad that it ensnares the prior art, rendering the claims invalid.

The specification, in view of the state of the art, makes clear that the alleged invention is limited to the "protective oxide layer" of a predetermined thickness, which, as taught by the patent, is between 30 Å to 80 Å for aluminum. The only difference between the then-conventional processes for making multilevel interconnects and the teachings of '177 patent is the thickness of the oxide layer that protects and the conditions by which it is formed.

The specification discusses, in the context of the prior art, that the claimed process steps are well known, including plasma ashing. [*See, e.g.*, Ex. 37, Col. 1:50-57.] The only difference is that the conventional method does not form the claimed "protective oxide layer." [*See id.*, Col. 1:50-2:2.] A review of the prior art reveals that even in the conventional method as described in the specification, an oxide layer would naturally form during plasma ashing.[16] For example, the prior art '141 patent cited by the examiner mentions the formation and subsequent removal of an oxide layer. [Ex. 40, Col. 5:9-13 ("Further, contaminants diffused from photoresist film 15 and a ***natural oxide film*** formed on wiring layer 13 which is the bottom surface of through hole 18 ***can be effectively removed*** by the second anisotropic etching process.").] Indeed, the '141 patent touted some of the same advantages as the '177 patent. [*Id.*, Col. 5:13-15 ("This ***improves*** the property of electrical connection ***between first and second wiring layers*** 13 and 19."); *see also* Ex. 37 Abstract ("high density and high speed semiconductor integrated circuit whose electrode characteristics ***between two wiring layers is***

[16] Indeed, an aluminum surface is known to always have an oxide layer in the presence of oxygen even without undergoing plasma ashing. [*See, e.g.*, Ex. 38, p. 66 ("For example, aluminum surfaces **always** have a thin aluminum oxide layer.").]

***improved***").] The claimed novelty of the '177 patent was the formation of the claimed "***protective*** oxide layer," not simply any "oxide layer."

The concept of "oxide layers" was amply understood in the prior art, especially in the context of aluminum and plasma ashing. Each of the following prior art references relates to forming multilayer interconnects and discloses that an oxide layer naturally forms during plasma ashing used to remove the remaining photoresist: JP61-134015, JP3-082127, JP2-133939, and JP61-140161.[17] In fact, the JP '015 reference discloses that an oxide film of about 25 Å is formed during plasma ashing. [Ex. 45, p. 3 ("[R]esidual photoresist film (3) is removed by ashing with oxygen plasma [and] [a]t this time, oxidizing film (4) of about 25 Å is formed in the diffusion window section exposed to oxygen plasma.").] The JP3-082127 discloses the formation of a 200 Å thick oxide film. [*See* Ex. 46, p. 4 ("[R]esist film (10) is removed by means of O2 ashing [and] natural oxide film (9) of about 200 Å thickness composed of alumina Al2O3 is formed on the surface in the section exposed at opening (5) of wiring film (3).").]

The only difference between the oxide layers formed by conventional methods, and the oxide layer taught and claimed in the '177 patent is that the '177 patent characterizes its oxide layer as being *protective*. The applicants further defined this term in their preliminary amendment to original claim 1 that had recited "forming an oxide layer" and added the word "protective" to claim "forming a protective oxide layer." [Ex. 49, p. 7.] Similarly, independent

---

[17] *See e.g.*, Ex. 41 at Abstract ("[R]esist layer 18 is ashed by an oxygen plasma and removed. During this an alumina film 20 is formed inside contact holes 16 Å wherein first wiring layer 14 is exposed."); Ex. 44, p. 3 ("[W]hile the resist ashing by oxygen plasma is carried out . . ., the Al2O3 film 28 is formed by the oxygen plasma on where the aluminum electrodes 23a, 23b are exposed.").

claim 8, added at the time of this amendment, also recites forming "a ***protective*** oxide layer" as opposed to merely an "oxide layer."

Accordingly, this claim term should only encompass the range of thickness that improves upon the conventional oxide layer and the conditions under which it is formed. As the '177 inventors taught, at 30 Å, the oxide layer was thick enough to provide protection for an aluminum layer, while at 80 Å, the oxide layer was able to be readily removed without a second etching step. [*See generally* Ex. 37; Ex. 46, pp. 4-5.] Thus in keeping with the teaching of the patent, the "protective oxide layer" must be "an oxide layer of a predetermined thickness." Moreover, in the case of an aluminum layer, the protective oxide layer must be "a thickness of 30 to 80 Å" to be within the scope of the invention. [*See, e.g.*, Ex. 37, Col. 2:63-3:2, 2:29-33, 4:13-15, 4:55-56.] *See Texas Instruments, Inc. v. United States Int'l Trade Comm'n*, 846 F.2d 1369, 1370 (Fed. Cir. 1988) ("The patentee's disclosure, the prosecution history, and the prior art still provide the background against which the scope of claims is determined.").

Even with a narrow construction, the validity of the '177 patent is seriously in doubt. Samsung's construction that undoubtedly renders the claims invalid should be rejected. *See, e.g.*, *Klein v. Russell*, 86 U.S. 433, 466 (1873); Rhine v. Casio, Inc., 183 F.3d 1342, 1345 (Fed. Cir. 1999) ("claims should be construed, if possible, to preserve their validity.").

3. "Removing Said Oxide Layer Before Forming a Second Conductive Layer on Said Exposed Top Surface of Said First Conductive Layer" (Claims 1 and 8)

| **ON Semiconductor** | **Samsung** |
|---|---|
| getting rid of the entire protective oxide layer before forming a second conductive layer such that the top surface of the first conductive layer is completely exposed | The meaning of this phrase requires no construction. To the extent a construction is necessary, the phrase should be construed as "removing the protective oxide layer." |

The ordinary meaning of the words of the claim support complete removal of the protective oxide layer. The ordinary meaning of "removing" means "get rid of," "to do away

with; eliminate." [Ex. 30, p. 1046.] The claim also specifically requires "removing said oxide layer before forming a second conductive layer ***on said exposed top surface of said first conductive layer***." [Ex. 37, Col. 4:3-5, 38-40.] Until the entire oxide layer is completely removed, the top surface of the first conductive layer cannot be exposed as required by this step of the claim.

The specification supports the plain meaning of this phrase. It teaches electrically connecting the first and second conductive layers to realize "minimum contact resistance drastically enhancing electrode characteristics between the two wiring layers." [ *Id.*, Col. 3:33-35.] This goal would be frustrated if the entire oxide layer were not removed because the oxide layer is an "insulator" that would increase contact resistance, or even prevent electrical conduction altogether. [*Id.*, Col. 3:2-3 ("an aluminum oxide layer 35, ***an insulation laye***r . . ").] The patent also describes that the aluminum oxide layer is removed with argon sputtering.[18] [Ex. 37, Col. 3:8-13; 4:57-59.] The use of sputtering is a well known etching technique that can remove all of the oxide layer. [*See e.g.*, Ex. 46, p. 5; Ex. 52, Col. 4:17-26.]

Finally, all of the conventional methods for forming low contact resistance multi-layer interconnects consistently teach removing the entire oxide layer prior to forming the interconnect. In fact, the complete removal of the entire oxide is so important that the JP '127 patent teaches undertaking a two step process to do so. [Ex. 46, pp. 4-5.] Numerous other prior art references relating to forming multilayer wiring consistently teach the importance of the complete removal of the oxide layer to provide low resistance interconnects with good electrical interconnection. [*See, e.g.*, Ex. 40, Col. 5:10-15 ("[A] natural oxide film formed on wiring layer

[18] Ex. C, p. 962 ("sputtering" in this context just means "dislocation of surface atoms of a material bombarded by high-energy atomic particles").

13 which is the bottom surface of through hole 18 can be effectively removed by the second anisotropic etching process."); JP2-133939 ("alumina film 20 is cleanly removed.")]; see *Vitronics*, 90 F.3d at 1584-85 (even when prior art is not cited in the specification or prosecution history, it may assist in ascertaining the meaning of a term to a person skilled in the art.)

Thus, the claim, the patent specification, and the prior art demonstrate that one of ordinary skill in the art would understand the term to require complete removal of the oxide layer.

4. "Photoresist"

| **ON Semiconductor** | **Samsung** |
|---|---|
| A light sensitive organic material that can be removed in oxygen plasma. | The meaning of this phrase requires no construction. To the extent a construction is necessary, the phrase should be construed as "a layer of photoresist material that selectively exposes an underlying layer." |

ON Semiconductor's construction is based on the ordinary meaning of photoresist as understood by one of ordinary skill in the art as well as both the intrinsic and extrinsic evidence while Samsung merely repeats the claim term.

The specification makes clear that a photoresist is removable by plasma ashing techniques. [Ex. 37, Col. 1:50-57, 3:61-63.] Oxygen plasma ashing, as generally known to those skilled in art, is suitable only for the removal of organic material. For instance, *Fundamentals of Semiconductor Processing Technologies* states that, in plasma ashing, "an oxygen plasma reacts readily with the organic resist but leaves inorganic films (such as oxide, nitride, polysilicon or metal) mostly intact." [Ex. 42, p. 211 (1995). Further, it is well established that "[p]hotoresists (or resists) are organic compounds whose solubility changes when exposed to ultraviolet light." [*Id.*, p. 201; *see also* Ex. 43, pp. 62-63 (1990) ("Photolithography is perhaps one of the most important processes in semiconductor device fabrication. It consists of transferring an image of a pattern onto the surface of the silicon slice. The basic scheme is to put down a layer of light

sensitive plastic called photoresist which is capable of withstanding the chemical conditions which are to be subsequently used.")] This reference further makes clear the "photo" aspects of photoresist. Namely, that it is a light sensitive material that can be developed into patterns in much the same way that photographic film is developed into images. [Ex. 42, pp. 201-11.] Thus, it follows that a photoresist is a light sensitive organic material that is removable in a plasma of oxygen.

5. "Exposed Top Surface" and "Expose a Top Surface of Said Conductive Layer"

| **ON Semiconductor** | **Samsung** |
|---|---|
| the uppermost surface of the unoxidized conductive layer is uncovered by the etching step | The meaning of these phrases require no construction. To the extent a construction is necessary, the phrases should be construed as:<br><br>***exposed top surface:*** "the exposed top surface of a layer of electrically conductive material."<br><br>***expose a top surface of said first conductive layer:*** "exposing a top surface of a layer of electrically conductive material [by etching]." |

ON Semiconductor provides a construction that properly construes the claim as consistently with what the inventors actually invented. *See Phillips*, 415 F.3d at 1322. Samsung, on the other hand, asserts that the phrases do not require construction and, even if they did, they should be construed without consideration of the context provided in the patent specification.

These terms require construction because they are not self-defining. Indeed, the parties' dispute regarding the meaning of these claim terms illustrates the ambiguity and need for claim construction. The ambiguity arises as a result of the naturally occurring oxide layer that forms on the surface of many materials and, in particular, aluminum.19 Such an oxide layer is not conductive but can be ambiguously referenced as part of the electrically conductive material.

19 *See supra* note 16 and accompanying text (discussing naturally occurring oxidation).

Thus, on its face, it is not clear whether "exposed top surface" refers to an oxidized or unoxidized top surface of the conductive layer. If this term is not construed, or is construed as Samsung proposes, then the "exposed top surface" will be overbroad and will necessarily encompass the prior art and the naturally occurring oxidation discussed in Section B(2)(c)(i), supra, thereby expanding the scope of claims 1 and 8 of the '177 patent beyond the actual invention, rendering the claims invalid.

A proper claim construction therefore should consider the intrinsic evidence to provide context for the "exposed top surface" and "expose a top surface of said first conductive layer." Notably, all the intrinsic evidence supports ON Semiconductor's proposed construction.[20] Samsung argues that no construction is necessary, but in support of its proposed construction cites to intrinsic evidence that actually supports ON Semiconductor's position.[21]

## CONCLUSION

For all of the reasons discussed above, ON Semiconductor's constructions should be adopted by the Court and Samsung's proposed constructions should be rejected.

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[20] *See*, e.g., Ex. 67, Figs. 1A-B, 2A-B; Abstract; col. 1:24-62 (same), 2:10-17, 3:23-28, 2:58-61 ("The wiring is composed of the second conductive layer, and another wiring layer are contacted through the contact hole 33."), 2:50-3:14, 3:2-21; claims 1 and 8.

[21] *See* D.I. 117 at Exs. pp. 32-33, 36 (Samsung citing to, inter alia, '177 Patent Abstract, Figs. 1A-B, 2A-B; col. 1:31-35, 1:41-62, 2:10-17, 2:58-61, 3:23-28; claims 1, 8, all of which support ON Semiconductor's proposed construction).

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**CERTIFICATE OF SERVICE**

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# EXHIBIT A

US005361001A

# United States Patent [19]

Stolfa

[11] Patent Number: 5,361,001

[45] Date of Patent: Nov. 1, 1994

[54] **CIRCUIT AND METHOD OF PREVIEWING ANALOG TRIMMING**

[75] Inventor: **David L. Stolfa**, Phoenix, Ariz.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **160,762**

[22] Filed: **Dec. 3, 1993**

[51] **Int. Cl.**[5] ..... **H03K 3/01**; H03B 1/04

[52] **U.S. Cl.** ..... **327/530**; 327/525; 327/312

[58] **Field of Search** ..... 307/202.1, 296.1, 547, 307/548

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| | | | |
|---|---|---|---|
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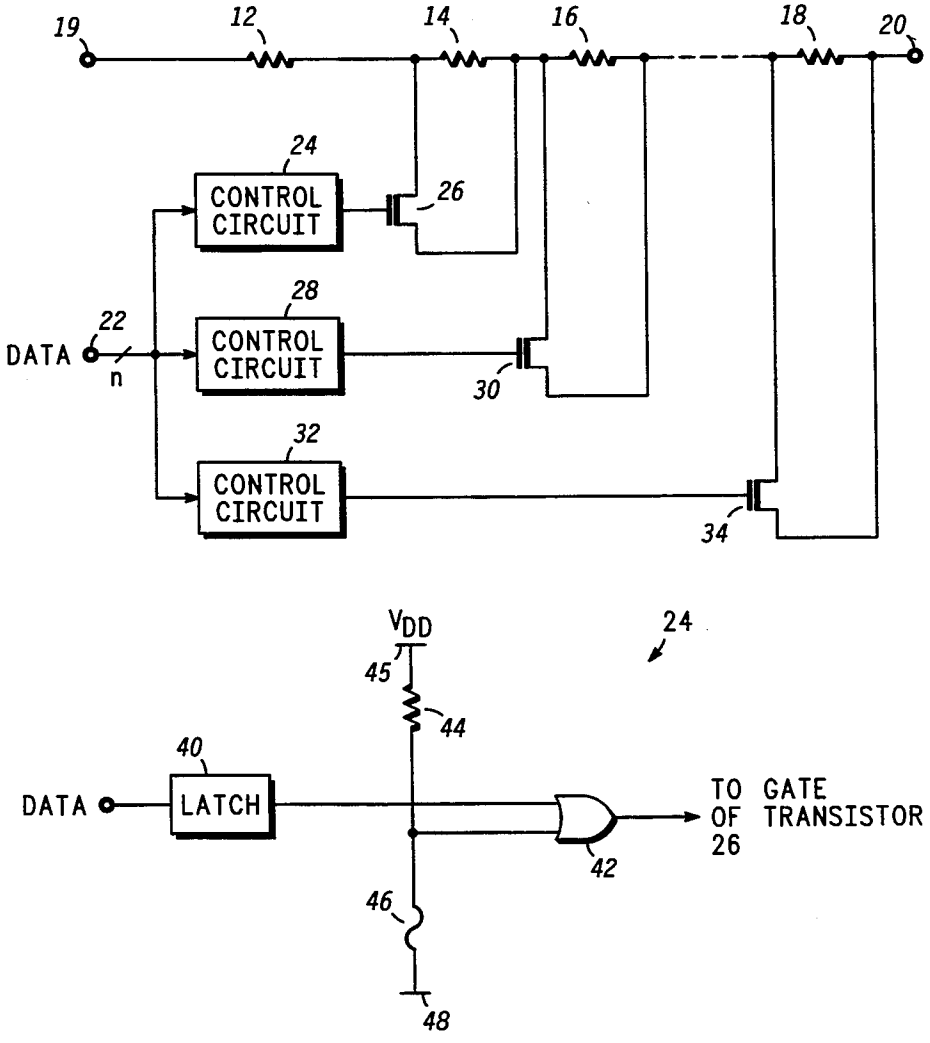
*Primary Examiner*—Margaret Rose Wambach
*Attorney, Agent, or Firm*—Robert D. Atkins

[57] **ABSTRACT**

An analog trim circuit enables and disables one or more serially connected passive elements for setting characteristics of the circuit. Each passive element has a transistor across its first and second conduction terminals operating in response to a control signal from a control circuit for enabling and disabling conduction through the associated passive element. The control circuits are responsive to a data signal for providing the control signals that enable and disable the conduction through the passive elements. The data signal allows a preview of the trimming results. The fuse in certain ones of the control circuits are blown to set the control signals to fixed values after removal of the data signal.

**7 Claims, 1 Drawing Sheet**



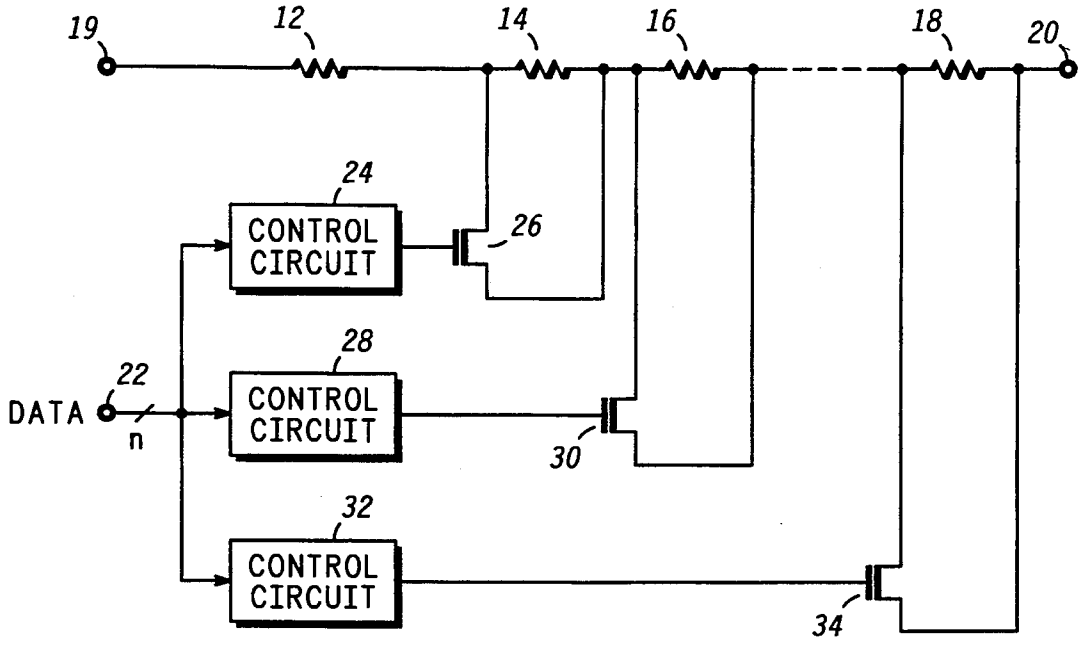
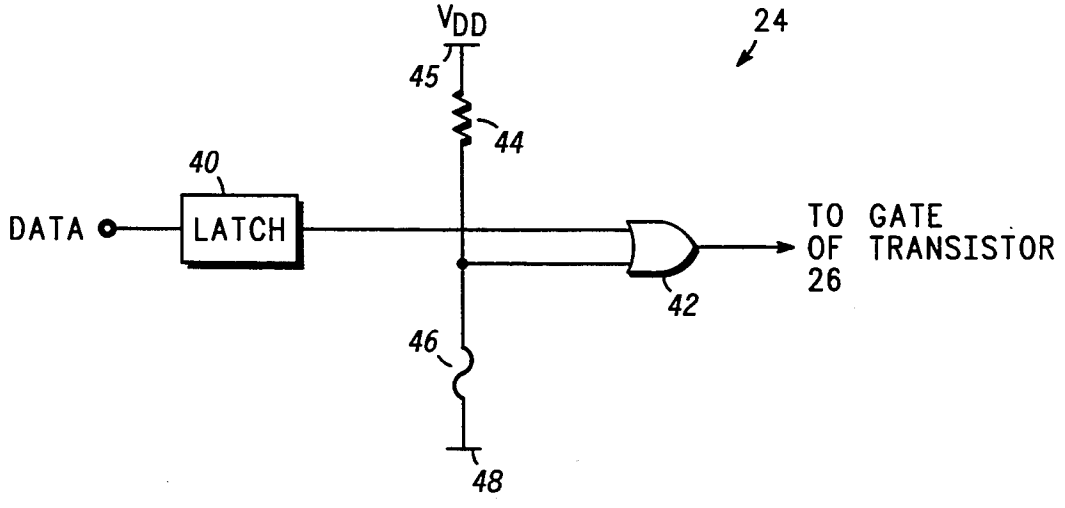

19
12
14
16
18
20
24
CONTROL CIRCUIT
26
28
CONTROL CIRCUIT
22
DATA
n
30
32
CONTROL CIRCUIT
34
10

FIG. 1

FIG. 2


$V_{DD}$
24
45
44
40
LATCH
DATA
TO GATE OF TRANSISTOR 26
42
46
48

# CIRCUIT AND METHOD OF PREVIEWING ANALOG TRIMMING

## BACKGROUND OF THE INVENTION

The present invention relates in general to analog trim circuits and, more particularly, to a technique of previewing the analog trim results before blowing a fuse to lock the trim in place.

In manufacturing analog integrated circuits, the basic building blocks are usually not accurately controlled by the manufacturing process as may be desired. For example, capacitors and resistors may have the wrong value, and MOS transistors may have the wrong gain setting. There are too many variables in the manufacturing process to yield absolute predictable results. Yet historically analog circuits often require very accurate voltage references, frequency references, and accurately ratioed elements.

To compensate for the process variability, many electronic circuits use analog trimming during test to set resistor values as necessary for proper operation of the circuit. A typical trimming technique utilizes a resistor ladder comprising a series of serially coupled resistors each in parallel with either a fuse or anti-fuse. A fuse is a device that is substantially an electrical short until it is blown open. An anti-fuse is an electrical open until blown when it becomes substantially an electrical short.

The fuse-blowing approach may take several forms, each with its own shortcomings. Laser fuses may be used directly across each resistor element in the ladder to enable and disable conduction through the resistor. During test, certain resistors are selected to open the shunt element thereby adding resistance to the serial path. The resistor ladder should be adjustable at wafer test over a range from say 10 to 2,560 ohms in 10 ohm increments.

The analog trimming may be performed iteratively, i.e. test, trim, test, trim, to measure the effect of the course trim and determine the necessary fine trimming. For iterative trimming, a laser trim system is typically installed on the wafer tester to alternately test and trim. However, one laser system per tester is very expensive. The laser is often in an idle state waiting for the tester. Moreover, if either the test system or laser breaks down both are inoperative.

An alternate approach is to use a zener anti-fuse across the resistor ladder. Such an element can be cheaply trimmed on the tester so that iterative testing can be done in one pass on the tester. Zener anti-fuses require large currents to program. Therefore, each anti-fuse requires its own external pad and probe card needle. This restricts the programming bit count to say 5–10 bits before the die area for test pads and complexity of the probe card requirements become prohibitive.

In general, iterative testing is a slow and expensive process. Consequently, many trimming techniques utilize only a single pass to evaluate which resistors in the serial string should be included to achieve the desired analog circuit operation. Thus, as result of a test measurement, the user blows the shunt fuse elements whereby the circuit is expected to operate as planned. The process of blowing the fuses typically involves laser trimming off-line from the test set to cut the poly material and open the shunt element. The circuit may be returned to the test set to verify proper trimming. If the subsequent testing should fail, the part is typically discarded since it is difficult to patch the shunt fuse elements.



Hence, a need exists for an iterative trimming to evaluate the results of test before permanently setting the trim.

## BRIEF DESCRIPTION OF THE DRAWING

FIG. **1** is a block diagram illustrating an analog trimming circuit; and

FIG. **2** is a schematic diagram illustrating the control circuit of FIG. **1**.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

An analog trim circuit is shown in FIG. **1** including a passive ladder network **10** comprising resistors **12, 14, 16** and **18** serially coupled between terminal **19** and terminal **20**. Resistor **12** is non-trimmable and provides the minimum ladder resistance ($R_{MIN}$). Resistors **14–18** are selected in an exponential series, such as 1280, 640, 320, 160, 80, 40, 20, and 10 ohms. Resistors **14–18** are passive elements each with first and second conduction terminals. Other passive elements may also be used in the trim circuit. A data signal is applied at terminal **22**. One bit of the data signal is applied to each of control circuits **20, 28** and **32**. An address signal selects the control circuit to latch one bit of the data signal.

Control circuit **24** provides a control signal to the gate of MOS transistor **26**. The drain and source of transistor **26** are coupled to first and second conduction terminals of resistor **14**. Likewise, control circuit **28** provides a control signal to the gate of MOS transistor **30** which has its drain and source coupled across resistor **16**. Control circuit **32** provides a control signal to the gate of MOS transistor **34**. The drain and source of transistor **34** are coupled across the first and second conduction terminals of resistor **18**. The effective resistance through resistor ladder **10** is thus temporarily set by transistors **26, 30** and **34** selectively enabling and disabling conduction through resistors **14–18** upon receiving a high state or low state of control signals from control circuits **24, 28** and **32**. With the above trimming scheme, the resistor ladder is controllable from $R_{MIN}$ to $R_{MIN}+2{,}560$ ohms assuming eight trimmable resistors in 256 possible 10 ohm increments.

Turning to FIG. **2**, further detail of control circuit **24** is shown. Control circuits **28** and **32** follow a similar construction and operation as described for control circuit **24**. The data signal is latched in latching circuit **40** for application to a first input of OR gate **42**. An address signal enables latching circuit **40** to latch the data bit. Resistor **44** is coupled between the second input of OR gate **42** and power supply conductor **45**. Power supply conductor **45** operates at a positive potential VDD such as 5 volts. Fuse **46** is coupled between the second input of OR gate **42** and power supply conductor **48** operating at ground potential. The output of OR gate **42** provides the control signal to the gate of transistor **26**. An alternate embodiment of control circuit **24** may replace OR gate **42** with a NAND gate while resistor **44** and fuse **46** exchange places in the circuit.

Trim circuits are used in a variety of applications. For example, a circuit may require a given frequency $f_o$ determined by an RC time constant such that the frequency is inversely proportional to RC. The resistance R and capacitance C should be selected such that the nominal process target values of sheet $\rho$ (resistance per

unit area) and capacitance per unit area yield the desired frequency $f_o$. However, the actual process values of resistance and capacitance may vary by 5%–10%. Thus, the trimmable resistor ladder **10** must be trimmed to compensate for any variation in sheet $\rho$ and capacitance per unit area.

During testing at wafer level, the circuit under test is exercised and any correction necessary to resistor ladder **10** is calculated by a binary search. Steps are taken to determine whether a resistor should be trimmed such that it is in the upper half or lower half of its trimmable range, i.e. determining if the most significant bit or largest resistor should be shorted or left to remain in resistor ladder **10**. With resistor ladder **10** trimmed to its most significant bit the circuit under test is again tested and a correction is calculated to determine if it should be trimmed to the upper half or lower half of the remaining trimmable range. As a result, the next most significant resistor is shorted or allowed to remain. The process continues until all trimmable resistors have been checked.

Consider the trimming operation during test where a logic one data signal is stored in latching circuit **40** of each of control circuits **24**, **28** and **32**. The output of each OR gate **42** goes high and enables transistors **26**, **30** and **34**. Resistors **14–18** are substantially shorted, i.e. disabling the conduction path through resistors **14–18**. The resistance of ladder **10** is equal to $R_{MIN}$.

To perform trim preview during test, the data signal to control circuit **24** is set to logic zero and stored in its latching circuit **40**. At wafer test all fuses are yet unblown so that all fuse inputs to the OR-gates are low. The control signal at the output of OR-gate **42** goes low and turns off transistor **26** to enable the conduction through resistor **14**. The resistance of ladder **10** increases to $R_{MIN}+R_{14}$, where $R_{14}$ is the value of resistor **14**. The effect of the added resistance on the operation of the circuit under test may be checked and verified by the tester. If more resistance is needed, the data signal to control circuit **28** may be set to logic zero. The control signal to transistor **30** goes low as described above for control circuit **24**. Transistor **30** turns off and enables the conduction through resistor **16**. The resistance of ladder **10** increases to $R_{MIN}+R_{14}+R_{16}$, where $R_{16}$ is the value of resistor **16**. Again, the effect of the added resistance on the operation of the circuit under test may be checked and verified by the tester. The process continues until the circuit under test operates as desired. Note at this point, the trimming process is temporary and dependent on the data signals to control circuits **24**, **28** and **32**. No fuses have yet been blown to lock in the trim. Thus, different combinations of resistors **14–18** may be previewed and checked to achieve optimal results.

An alternate trim approach could initially set the data signals to logic zero in control circuits **24**, **28** and **32**. The output of each OR gate **42** goes low and disables transistors **26**, **30** and **34**. The shunt elements **26**, **30** and **34** are substantially opened, i.e. enabling conduction through resistors **14–18**, thereby making ladder **10** resistance maximum. The testing preview involves setting the data signals to logic one and iteratively enabling transistors **26**, **30** and **34** to disable conduction through resistors **14–18** and reduce resistance in ladder **10**. The process continues until the circuit under test operates as desired. Again, the trimming process is temporary and dependent on the data signals to control circuits **24**, **28** and **32**. No fuses have yet been blown to lock in the trim. Different combinations of resistors **14–18** may be tried and checked to achieve optimal results.

Another embodiment of the present invention is to configure the resistor ladder with the resistors in parallel and the control transistors in series with each resistor.

For the circuits under test that functionally pass, the bit pattern of trim is recorded in a file by wafer and die site. The file accompanies the wafer to a laser fuse system where the selected fuses **46** are blown. Once the appropriate fuses are blown, the latches in the control circuits are set to logic zero so that the state of the fuses alone determines the state of the control signal and therefore the permanent trim. The control signals from control circuits **24**, **28** and **32** are thus set to a fixed value by blowing the selected fuses **46** in the control circuits after removal of the data signal at terminal **22**.

The fuses are generally doped polycrystalline silicon films sometimes silicided polycrystalline silicon films in the range of 10 to 500 ohms. The polysilicon film is usually made in the shape of a polysilicon resistor with a width five to ten times its length. The ends of the fuses are connected by metal interconnects to the relevant circuitry. The fuse usually has most or all overlying oxide layers removed. With the use of on-die alignment marks the laser beam of approximately 1 $\mu$m–2 $\mu$m beam width is focused on the center of the fuse. The laser beam is a pulsed signal of such an energy that the polysilicon is vaporized and the fuse is severed and therefore permanently no longer conductive.

A key feature of the present invention is to preview trimming at wafer test to provide an economical means of iteratively trimming the resistive ladder using data provided by the tester. A data signal selectively trims the resistor ladder. The trimming is temporary and may be modified with different data signals to achieve optimal results. When the proper pattern of trim bits is determined for each individual circuit under test, that data is recorded and transferred off-line to the laser trimmer along with the wafer. The laser trim system blows the appropriate fuses for each circuit under test according to the pattern previously determined by testing various trimming options. Once the appropriate fuses are blown, the latches in the control circuits are set to logic zero so that the state of the fuses alone determines the state of the control signal and therefore sets the permanent trim. The preview trimming process allows optimization of the bit pattern for trimming before the actual laser trimming. Furthermore, the testing and the fusing systems may remain separate without requiring multiple passes through each.

While specific embodiments of the present invention have been shown and described, further modifications and improvements will occur to those skilled in the art. It is understood that the invention is not limited to the particular forms shown and it is intended for the appended claims to cover all modifications which do not depart from the spirit and scope of this invention.

I claim:

1. An analog trim circuit, comprising:

a passive element having first and second conduction terminals;

first means coupled across said passive element and operating in response to a control signal for enabling and disabling conduction through said passive element, said first means includes a transistor having a gate, a drain and a source, said drain being coupled to said first conduction terminal, said

source being coupled to said second conduction terminal, said gate being coupled for receiving said control signal; and

second means responsive to a data signal for providing said control signal to said first means to enable and disable said conduction through said passive element, said second means setting said control signal to a fixed value after removal of said data signal.

2. The analog trim circuit of claim 1 wherein said passive element includes a first resistor coupled between said first and second conduction terminals.

3. The analog trim circuit of claim 2 wherein said second means includes:

a latching circuit having an input coupled for receiving said data signal and having an output;

a logic gate having first and second inputs and an output, said first input being coupled to said output of said latching circuit, said output being coupled for providing said control signal;

a second resistor coupled between a first power supply conductor and said second input of said logic gate; and

a fuse coupled between said second input of said logic gate and a second power supply conductor.

4. A method of analog trimming, comprising the steps of:

enabling conduction through a passive element in response to a first state of a control signal;

disabling conduction through said passive element in response to a second state of said control signal;

activating said control signal in response to a data signal to enable and disable said conduction through said passive element, said activating step including the steps

(a) latching said data signal, and

(b) logically combining said data signal with a logic signal for providing said control signal; and

setting said control signal to a fixed value after removal of said data signal.

5. The method of claim 4 wherein said setting step includes the steps of:

removing said data signal; and

blowing a fuse to set said control signal at said fixed value.

6. An analog trim circuit, comprising:

a passive element having first and second conduction terminals;

a transistor having a gate, a drain and a source, said drain being coupled to said first conduction terminal, said source being coupled to said second conduction terminal, said gate being coupled for receiving a control signal;

a latching circuit having an input coupled for receiving a data signal and having an output;

a logic gate having first and second inputs and an output, said first input being coupled to said output of said latching circuit, said output being coupled for providing said control signal;

a first resistor coupled between a first power supply conductor and said second input of said logic gate; and

a fuse coupled between said second input of said logic gate and a second power supply conductor.

7. The analog trim circuit of claim 6 wherein said passive element includes a first resistor coupled between said first and second conduction terminals.

* * * * *

# EXHIBIT B

US006362644B1

(12) **United States Patent**
**Jeffery et al.**

(10) **Patent No.: US 6,362,644 B1**
(45) **Date of Patent: Mar. 26, 2002**

(54) **PROGRAMMABLE TERMINATION FOR INTEGRATED CIRCUITS**

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(73) Assignee: **Semiconductor Components Industries LLC**, Phoenix, AZ (US)

( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(22) Filed: **Aug. 1, 2000**

(51) **Int. Cl.**[7] ..... **H03K 17/16**
(52) **U.S. Cl.** ..... **326/30**; 326/101
(58) **Field of Search** ..... 326/30, 62, 63, 326/101; 327/333, 564, 565

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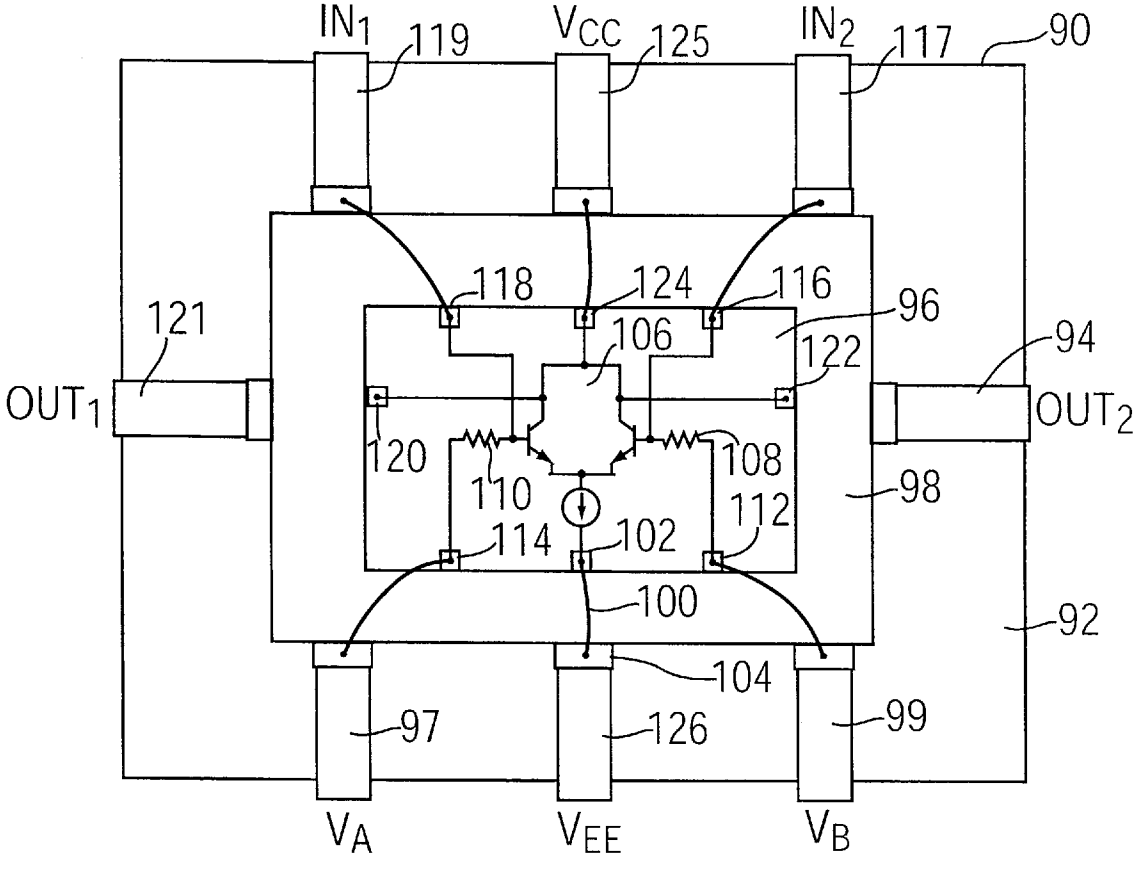
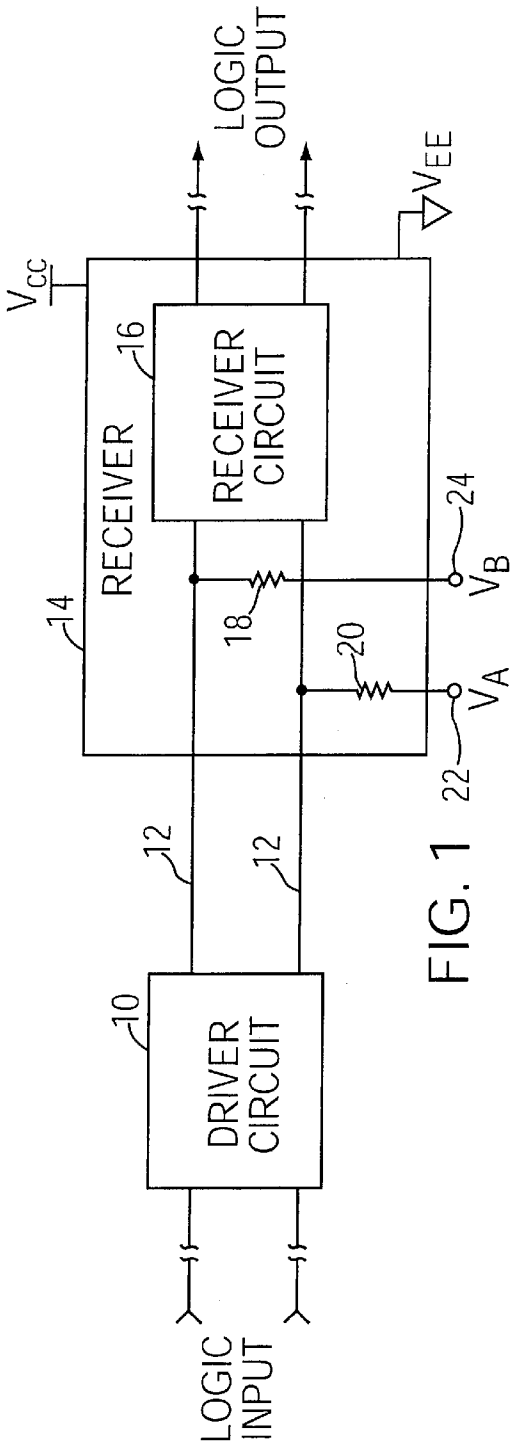
*Primary Examiner*—Tuan T. Lam

(57) **ABSTRACT**

A receiver circuit **(16)** is programmable to operate with different logic family driver circuits **(10)**. The receiver circuit has two external configuration pins **(22,) 24)** that are configured to provide the necessary termination for the type of logic family driver circuit used. To terminate the receiver circuit **(16)** for an ECL application will require first and second configuration pins **(22,24)** are connected to $V_{CC}$—2 volts. To terminate the receiver circuit **(16)** for a CML application will require the first configuration pin **(22)** and the second configuration pin **(24)** are connected to $V_{CC}$. LVDS termination for the receiver circuit **(16)** requires the first configuration pin **(22)** and the second configuration pin **(24)** are connected together. The configuration pins are external to a semiconductor package **(14)** housing the receiver circuit.

**16 Claims, 3 Drawing Sheets**

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$V_{EE}$
$V_{CC}$
RECEIVER
16
RECEIVER CIRCUIT
14
18
20
24
$V_B$
$V_A$
22
12
12
10
DRIVER CIRCUIT
LOGIC INPUT

FIG. 1

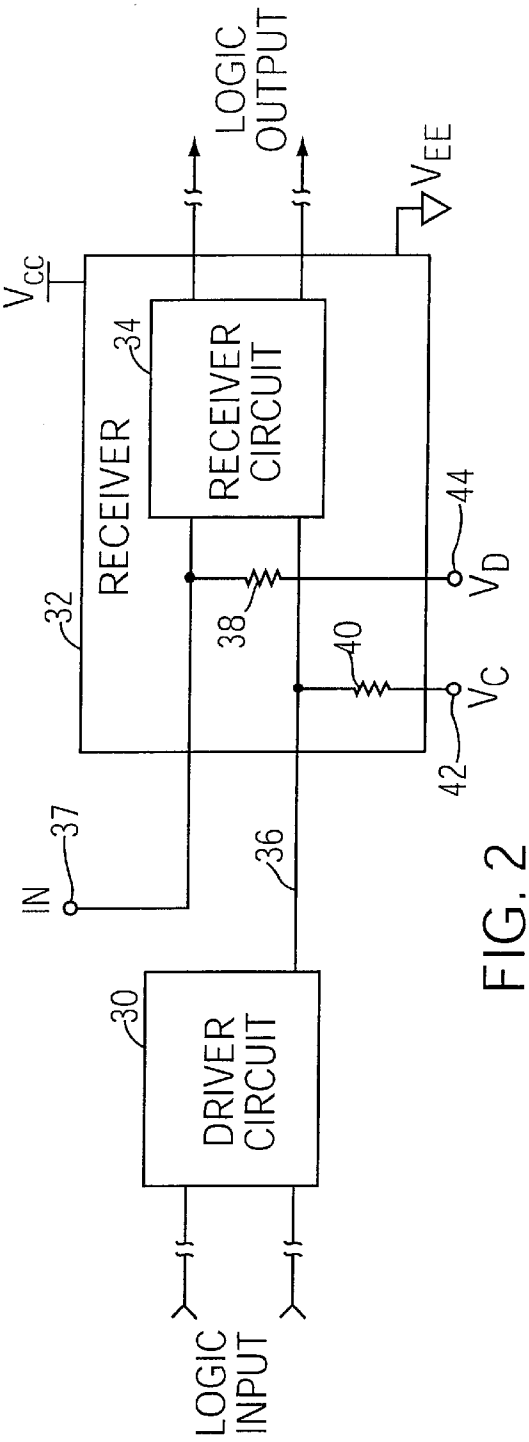

LOGIC OUTPUT
$V_{EE}$
$V_{CC}$
RECEIVER
34
RECEIVER CIRCUIT
32
38
40
44
$V_D$
$V_C$
42
IN
37
36
30
DRIVER CIRCUIT
LOGIC INPUT

FIG. 2

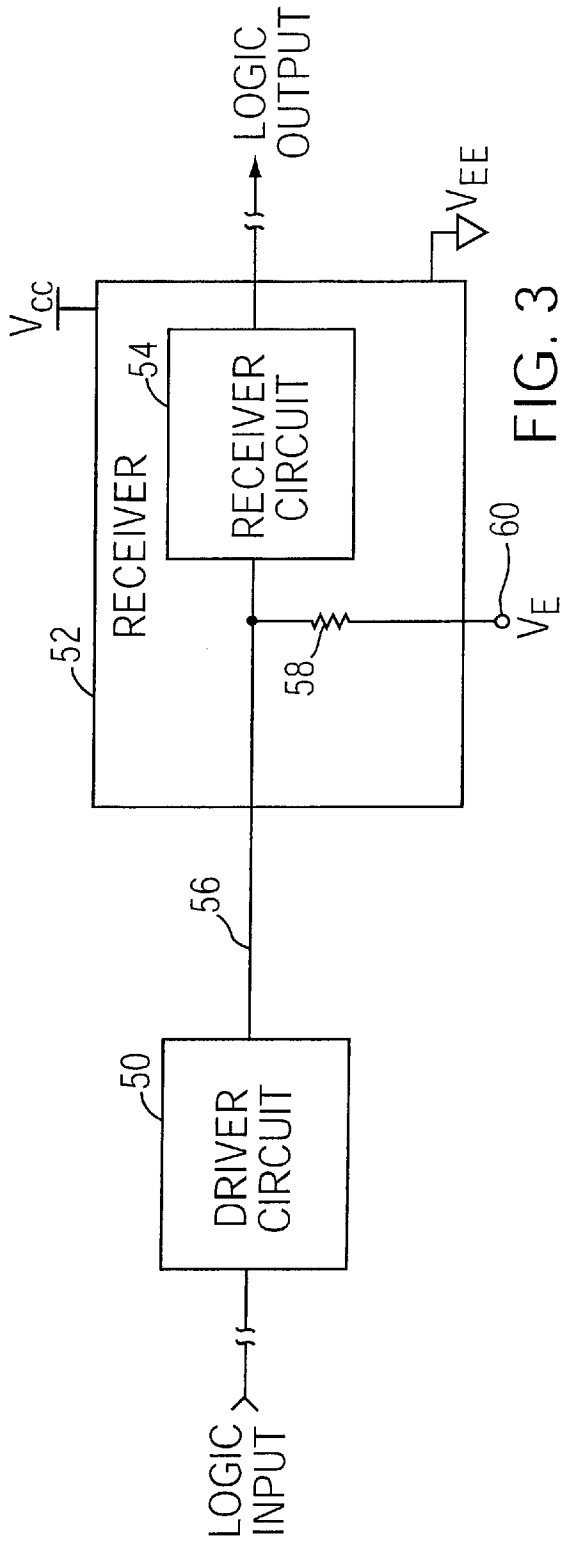

LOGIC OUTPUT
$V_{EE}$
$V_{CC}$
RECEIVER
54
RECEIVER CIRCUIT
52
60
$V_E$
58
56
50
DRIVER CIRCUIT
LOGIC INPUT

FIG. 3

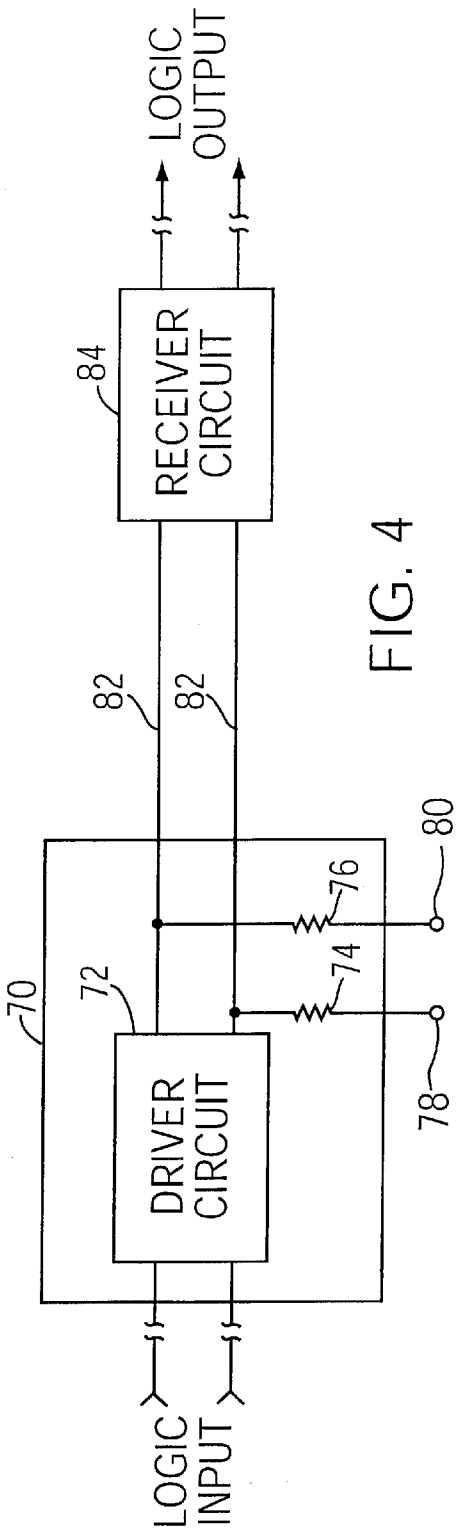

LOGIC OUTPUT
84
RECEIVER CIRCUIT
82
82
80
76
74
70
72
78
DRIVER CIRCUIT
LOGIC INPUT

FIG. 4

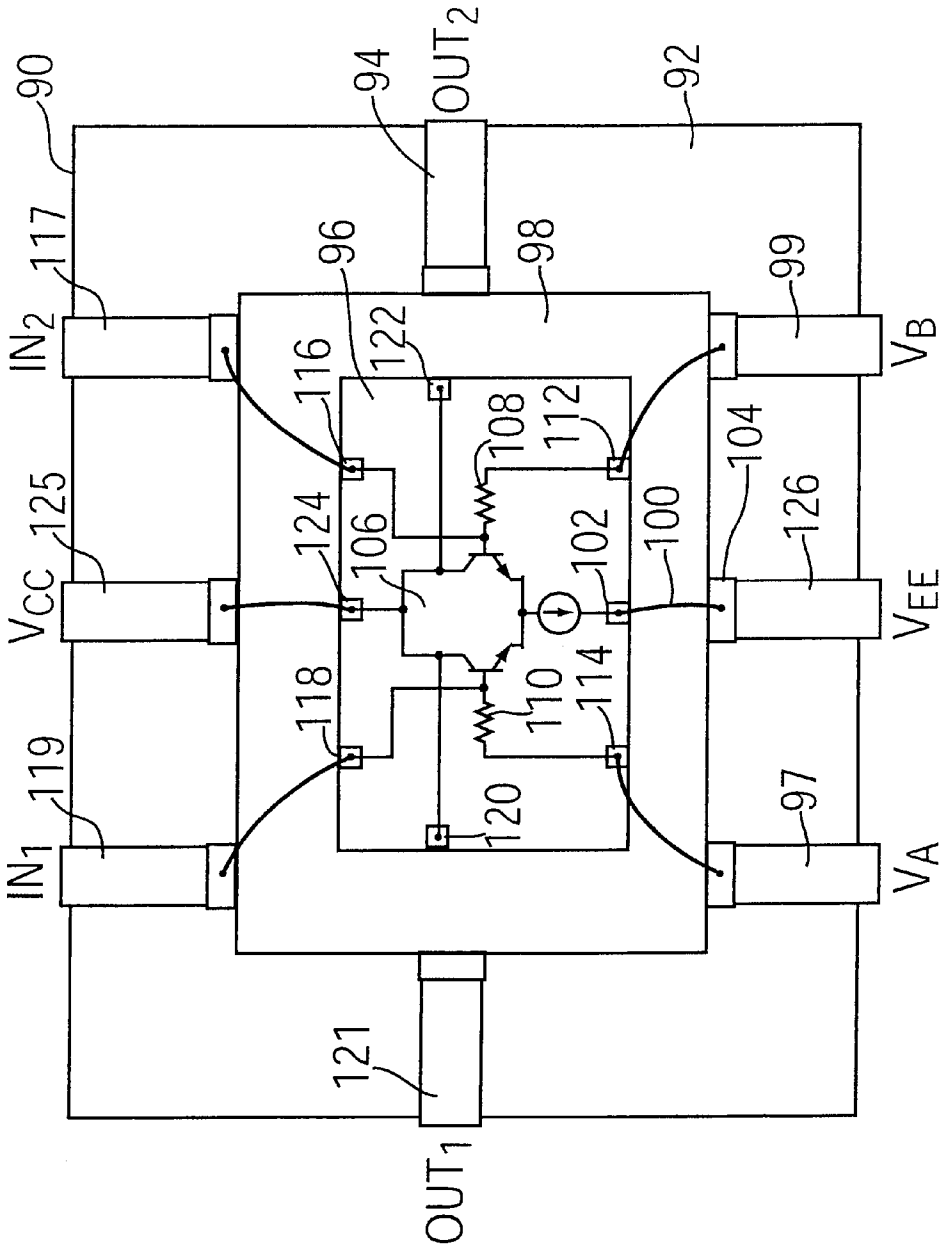

90
94
OUT2
92
117
96
98
99
IN2
VB
116
122
108
112
104
125
124
106
102
100
126
VCC
VEE
118
110
114
119
120
97
IN1
VA
121
OUT1

FIG. 5

# PROGRAMMABLE TERMINATION FOR INTEGRATED CIRCUITS

## BACKGROUND OF THE INVENTION

The present invention relates in general to electronic circuits and, more particularly, to logic circuits.

Many logic family applications have logic devices that operate within a mixed signal environment. The logic devices have logic drivers that may communicate with a logic receiver of a different logic family type. Typically, different logic family devices communicate with each other using translators to convert, for example, an ECL signal from the logic driver to a CMOS signal received at the logic receiver. A different type of translator is required for each type of logic driver and logic receiver used within the mixed signal environment. In addition, systems usually have an external termination scheme on an interconnect transmission line between the logic driver and logic receiver so the logic receiver circuit is terminated to receive the specific logic driver family type. The termination is a resistance that provides a termination for the logic device through to a voltage source Vtt. The voltage source Vtt is typically different for each logic family application. The resistance is typically chosen to equal the impedance of the interconnect transmission line to help reduce interconnect signal distortion. It is more of an advantage to have terminations as close as possible to the logic receiver circuit to help reduce interconnect signal distortion even more. Also, prior art termination schemes typically require different termination connections are used for each type of logic family device. For example, to use an ECL logic device requires a 50 ohm termination to a Vtt voltage source. A CML logic device may require termination through a resistance to a different voltage source. Most prior art logic family devices also have the termination resistors hard-wired to a circuit board making it difficult to change terminations for different logic family applications.

Hence, it is desired to have a logic receiver circuit that is programmable to allow the logic receiver circuit to communicate with different logic family driver circuits. Furthermore, it is desirable to have the terminations internal to the logic receiver circuit package so the terminations are close to the receiving circuit to help eliminate transmitted signal noise. The invention disclosed herein will address the above problems.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic diagram of a driver and receiver circuit in a differential configuration;

FIG. **2** is a schematic diagram of a driver and receiver circuit in a single-ended configuration;

FIG. **3** is a schematic diagram of a driver and receiver circuit in a modified single-ended configuration;

FIG. **4** is a schematic diagram of a driver and receiver circuit in a differential configuration with driver circuit terminations; and

FIG. **5** is a schematic diagram of a receiver circuit showing semiconductor and package connections.

## DETAILED DESCRIPTION OF THE PREFERED EMBODIMENT

FIG. **1** illustrates an embodiment of a driver circuit and a receiver circuit system used in a differential configuration. The differential configuration receives a logic input signal at driver circuit **10**. Driver circuit **10** is a device from a typical



logic family, e.g. ECL, CML, LVDS, CMOS, and TTL, or can be an analog driver circuit. The primary purpose of driver circuit **10** is to provide a signal boost for the logic input signal. At the output to driver circuit **10** is differential line **12** which transmits a differential signal from driver circuit **10** to receiver package **14**. Receiver package **14** is a semiconductor package housing receiver circuit **16**. $V_{CC}$ and $V_{EE}$ are power supply potentials to receiver package **14** providing power to receiver circuit **16**. Receiver circuit **16** receives a differential input signal on differential line **12** and provides a logic output signal. Receiver circuit **16** is typically a differential receiver circuit amplifier manufactured as a semiconductor die. Receiver circuit **16** and receiver package **14** are an integrated receiver circuit.

Differential line **12** is terminated with load element **18** and load element **20**. Load element **18** is connected to configuration pin **24** and load element **20** is connected to configuration pin **22**. Load elements **18**, **20** are resistors contained within receiver package **14** having a resistance of 50, 75, or 100 ohms. Configuration pins **22**, **24** are external pins connected to receiver package **14** and are programmable so receiver circuit **16** can communicate with different logic family drivers. To program configuration pins **22**, **24**, the pins are terminated using a configuration which is dependent on the desired logic family application. The configuration of receiver circuit **16** is controlled by connecting configuration pin **22** ($V_A$) and configuration pin **24** ($V_B$) as follows.

| | |
|---|---|
| ECL: | $V_A = V_B = V_{cc} - 2$ volts |
| CML: | $V_A = V_B = V_{CC}$ |
| LVDS: | $V_A$ connected to $V_B$ |

For example, to terminate receiver circuit **16** for an ECL application requires configuration pin **22** ($V_A$) and configuration pin **24** ($V_B$) are connected to receive configuration signal, $V_{CC}$–2 volts. To terminate receiver circuit **16** for an CML application requires configuration pin **22** ($V_A$) and configuration pin **24** ($V_B$) are connected to to receive configuration signal, $V_{CC}$. LVDS termination for receiver circuit **16** requires configuration pin **22** ($V_A$) and configuration pin **24** ($V_B$) are connected together. Termination of the configuration pins **22**, **24** is done external to receiver package **14**.

FIG. **2** illustrates an embodiment of a driver circuit and a receiver circuit system used in a single-ended configuration. The single-ended configuration receives a logic input signal at driver circuit **30**. Driver circuit **30** is a device from a typical logic family, e.g. ECL, CML, LVDS, CMOS, and TTL, or can be an analog driver circuit. Driver circuit **30** provides a signal boost for the logic input signal. Line **36** is connected to the output of driver circuit **30** to transmit a signal from driver circuit **30** to receiver package **32**. Receiver package **32** is a semiconductor package for receiver circuit **34**. $V_{CC}$ and $V_{EE}$ are power supply potentials to receiver package **32** providing power to receiver circuit **34**. Receiver circuit **30** is typically a differential receiver circuit amplifier manufactured as a semiconductor die. Receiver circuit **30** and receiver package **32** are an integrated receiver circuit.

Receiver circuit **34** receives two input signals: an information signal from driver circuit **30** on terminal **36**, and control signal IN on terminal **37**. Receiver circuit **34** is terminated at terminal **36** with load element **40**, and at terminal **37** with load element **38**. Load element **38** is connected to configuration pin **44** and load element **40** is connected to configuration pin **42**. Load elements **38**, **40** are

resistors contained within receiver package **32** having a resistance of 50, 75, or 100 ohms. Configuration pins **42**, **44** are external pins connected to receiver package **32** and are programmable so receiver circuit **34** can communicate with different logic family drivers. Configuration pins **42**, **44** are programmed by terminating the pins using a configuration which is dependent on the desired logic family application. The configuration of receiver circuit **34** is controlled by connecting configuration pin **42** ($V_C$) and configuration pin **44** ($V_D$) as follows.

| | |
|---|---|
| ECL: | $V_C = V_{CC}$ - 2 volts<br>$V_D$ = open<br>IN = $V_{BB}$ |
| CMOS: | $V_C$ = open<br>$V_D$ = open<br>IN = $V_{CC}/2$ |
| TTL: | $V_C$ = open<br>$V_D$ = open<br>IN = 1.5 volts |

$V_{BB}$ is typically the middle of an output swing to an ECL output. To terminate receiver circuit **34** for an ECL application requires configuration pin **42** ($V_C$) is connected to receive configuration signal, $V_{CC}$–2, configuration pin **44** ($V_D$) is devoid of a configuration signal, i.e. is left open, and terminal **37** is connected to receive control signal, $V_{BB}$. To terminate receiver circuit **34** for a CMOS application requires configuration pin **42** ($V_C$) and configuration pin **44** ($V_D$) are devoid of a configuration signal, and terminal **37** is connected to receive control signal, $V_{CC}/2$. TTL termination for receiver circuit **34** requires configuration pin **42** ($V_C$) and configuration pin **44** ($V_D$) are devoid of a configuration signal, and terminal **37** is connected to receive control signal, 1.5 volts. Termination of the configuration pins **42**, **44** is done external to receiver package **32**.

FIG. **3** illustrates an embodiment of a driver circuit and a receiver circuit system used in a modified single-ended configuration. The single-ended configuration receives a logic input signal at driver circuit **50**. Driver circuit **50** is a device from a typical type of logic family, e.g. ECL, CML, LVDS, CMOS, and TTL, or can be an analog driver circuit. Driver circuit **50** provides a signal boost for the logic input signal. Receiver package **52** receives a drive signal on line **56** from driver circuit **50**. Receiver package **52** is a semiconductor package for receiver circuit **54**. $V_{CC}$ and $V_{EE}$ are power supply potentials to receiver package **52** providing power to receiver circuit **54**. Receiver circuit **54** is terminated with load element **58** which is connected to configuration pin **60**. Load element **58** is a resistor contained within receiver package **52** having a resistance of 50, 75, or 100 ohms. Configuration pin **60** is an external pin connected to receiver package **52** that is programmable so receiver circuit **54** can communicate with different logic family drivers. Configuration pin **60** is programmed by terminating the pin using a configuration which is dependent on the desired logic family application. The configuration of receiver circuit **54** is controlled by connecting configuration pin **60** ($V_E$) as follows.

| | |
|---|---|
| ECL: | $V_E = V_{CC} - 2$ |
| CML: | $V_E = V_{CC}$ |
| LVDS: | $V_E$ = open |

To terminate receiver circuit **54** for an ECL application requires that configuration pin **60** ($V_E$) is connected to receive configuration signal, $V_{CC}$–2. For a CML application, receiver circuit **54** is terminated with configuration pin **60** ($V_E$) connected to receive configuration signal, $V_{CC}$. LVDS termination for receiver circuit **54** requires that configuration pin **60** ($V_E$) be left open. Termination of the configuration pin **60** is done external to receiver package **52**.

FIG. **4** illustrates a differential configuration similar to FIG. **1**, except termination is done on driver package **70**. Driver circuit **72** is terminated at load element **74** and load element **76**. Load element **74**, **76** are resistors contained within driver package **70** having a value of 50, 75, or 100 ohms. Configuration pin **78** and configuration pin **80** are configured similar to table shown for the differential configuration in FIG. **1**. Driver circuit **72** provides an output signal on differential line **82** to receiver circuit **84**.

FIG. **5** illustrates a detailed schematic of the differential configuration in FIG. **1**. Semiconductor package **90** houses a leadframe **92** with metal leads similar to lead **94** which provide input and output signals. The input and output signals consist of differential input logic signals $IN_1$, and $IN_2$, differential output logic signals $OUT_1$, and $OUT_2$, power supply signals $V_{CC}$ and $V_{EE}$, and configuration signals $V_A$ and $V_B$ on configuration pins **97**, **99** respectfully. Semiconductor die **96** is attached to flag **98** which is attached to leadframe **92**. Bond wire **100** is attached to bond pad **102** on semiconductor die **96** to provide electrical contact to bond pad **104** for the $V_{EE}$ signal. All other input and output signals have the same bond wire configuration to provide electrical contact. The wire bonding technology used is typically a bump type technology or a ball grid array (BGA) technology. The differential configuration typically has differential amplifier **106** for receiver circuit **16** of FIG. **1**. Load elements **108**, **110** are connected to bond pads **112**, **114** respectfully to provide an electrical connection to configuration signals $V_B$ and $V_A$. The differential signal from logic circuit **10** of FIG. **1** is received at lead **119** ($IN_1$) and lead **117** ($IN_2$) which has electrical contact to bond pads **118**, **116** on semiconductor die **96**, and to differential amplifier **106**. The logic output signal from receiver circuit **16** of FIG. **1** is coupled from differential amplifier **106**, electrical contact is made to bond pads **120**, **122** on semiconductor die **96**, and the signals are coupled to leads **121**. ($OUT_1$) and **94** ($OUT_2$) respectfully. Power supply is received at leads **125** ($V_{CC}$) and **126** ($V_{EE}$) making electrical contact to differential amplifier **106** through bond pads **124**, **102** respectively.

An alternative method to provide termination to any of the above embodiments is to use a switch between the termination (load) elements and the (configuration) termination signals. For example, FIG. **1** has external (configuration) termination pins **22**, **24** which are configured to receive different termination signals depending on the logic family application. A switch can be used to programmably connect termination pins **22**, **24** to $V_{CC}$–2 for an ECL logic family application, or to $V_{CC}$ for a CML logic family application. The switch can provide programmability for the termination signals to any of the previous configurations outlined herein.

Thus, a technique for generating multiple input termination options on a single integrated circuit is disclosed. A receiver circuit is programmable to configure different termination connections which allow the receiver circuit to communicate with a driver circuit from a different logic family. The receiver circuit has at least one external configuration pin that is configured to provide the necessary termination for the type of logic family driver circuit used. The configuration pin is external to a semiconductor package housing the receiver circuit. Having configuration pins external to the semiconductor package provides for easy

portability among different logic families, and easy termination options which require no additional translators to operate a mixed logic family system.

What is claimed is:

**1**. An integrated logic circuit having a differential input receiving a differential signal, comprising:

a receiver having first and second inputs coupled for receiving the differential signal;

a semiconductor package for housing the receiver, having first and second pins respectively coupled to the first and second inputs of the receiver, and a supply pin coupled to the receiver for providing a power supply potential;

a first termination element housed in the semiconductor package and coupled between the first input of the receiver and a first programmable configuration pin of the semiconductor package; and

a second termination element housed in the semiconductor package and coupled between the second input of the receiver and a second programmable configuration pin of the semiconductor package, wherein the first and second programmable configuration pins receive first and second termination signals to configure termination for the logic circuit.

**2**. The integrated logic circuit of claim **1**, wherein the first and second termination elements comprise resistors.

**3**. A method of configuring a receiver circuit using first and second configuration signals, and receiving first and second input signals to the receiver circuit, comprising:

coupling an information signal on the first input to the receiver circuit;

coupling a control signal on the second input to the receiver circuit;

providing a first programmable configuration pin of a semiconductor package housing the receiver circuit;

connecting a first load element between the first input of the receiver circuit and the first programmable configuration pin;

providing a second programmable configuration pin of a semiconductor package housing the receiver circuit; and

connecting a second load element between the second input of the receiver circuit and the second programmable configuration pin.

**4**. The method of claim **3**, wherein the first and second programmable configuration pins receive a configuration selected from the group consisting of the first configuration signal, the second configuration signal, and devoid of the first and second configuration signals.

**5**. The method of claim **3**, wherein the second input receives a control signal selected from the group consisting of a first control signal, a second control signal, and a third control signal.

**6**. An integrated circuit, comprising:

a semiconductor package having first and second pins respectively adapted for receiving first and second data signals, third and fourth pins for respectively receiving first and second termination signals, and a supply pin coupled for receiving a power supply voltage; and

a semiconductor die housed in the semiconductor package for operating from the power supply voltage, and having a first load element coupled between the first and third pins to terminate the first data signal, and a second load element coupled between the second and fourth pins to terminate the second data signal.

**7**. The integrated circuit of claims **6**, wherein the first and second load elements are resistors.

**8**. The integrated circuit of claim **6**, wherein the semiconductor die includes a receiver circuit having first and second inputs coupled to the first and second pins, respectively.

**9**. The integrated circuit of claim **6**, wherein the semiconductor die includes a driver circuit having first and second outputs coupled to the first and second pins, respectively.

**10**. The integrated circuit of claim **6**, wherein the first data signal is from a first logic family, and the third pin is coupled for receiving a first termination voltage characteristic of the first logic family.

**11**. The integrated circuit of claim **10**, wherein the second data signal is from a second logic family, and the fourth pin receives a second termination voltage of the second logic family.

**12**. A method of operating an integrated circuit, comprising the steps of:

applying first and second logic signals to first and second pins, respectively, of a semiconductor package of the integrated circuit; and

loading the first and second logic signals with first and second load elements, respectively, of the integrated circuit, where the first and second load elements are coupled to third and fourth pins of the semiconductor package to provide a programmable termination for the first and second logic signals.

**13**. The method of claim **12**, wherein the first and second logic signals function as a differential signal and the third and fourth pins are for coupling together to terminate the differential signal.

**14**. The method of claim **12**, wherein the first and second logic signals are specified in accordance with first and second logic families and the third and fourth pins are coupled to first and second configuration signals of the first and second logic families, respectively.

**15**. The method of claims **14**, wherein the first and second logic signals are ECL signals referenced to a supply voltage, and the first and second configuration signals have values equal to the supply voltage minus about two volts.

**16**. The integrated logic circuit of claim **12**, further comprising the step of applying a power supply voltage to a fifth pin of the semiconductor package to bias the integrated circuit.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

# CERTIFICATE OF CORRECTION

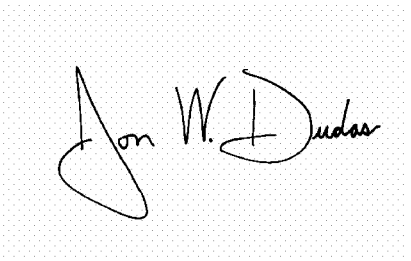
PATENT NO. : 6,362,644 B1 
DATED : March 26, 2002
INVENTOR(S) : Philip A. Jeffery and Stephen G. Shook

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 6,
Line 53, please change "The intergrated logic circuit of" to -- The method of --.

Signed and Sealed this

Third Day of May, 2005



JON W. DUDAS
*Director of the United States Patent and Trademark Office*

# EXHIBIT C

US005563594A

# United States Patent [19]

**Ford et al.**

[11] **Patent Number: 5,563,594**

[45] **Date of Patent: Oct. 8, 1996**

[54] **CIRCUIT AND METHOD OF TIMING DATA TRANSFERS**

[75] Inventors: **David K. Ford**, Gilbert; **Bernard E. Weir, III**, Chandler, both of Ariz.

[73] Assignee: **Motorola**, Schaumburg, Ill.

[21] Appl. No.: **298,715**

[22] Filed: **Aug. 31, 1994**

[51] **Int. Cl.**[6] ..... **H03M 9/00**

[52] **U.S. Cl.** ..... **341/100**; 341/101; 327/279

[58] **Field of Search** ..... 341/100, 101; 326/93; 327/160, 175, 265, 279

[56] **References Cited**

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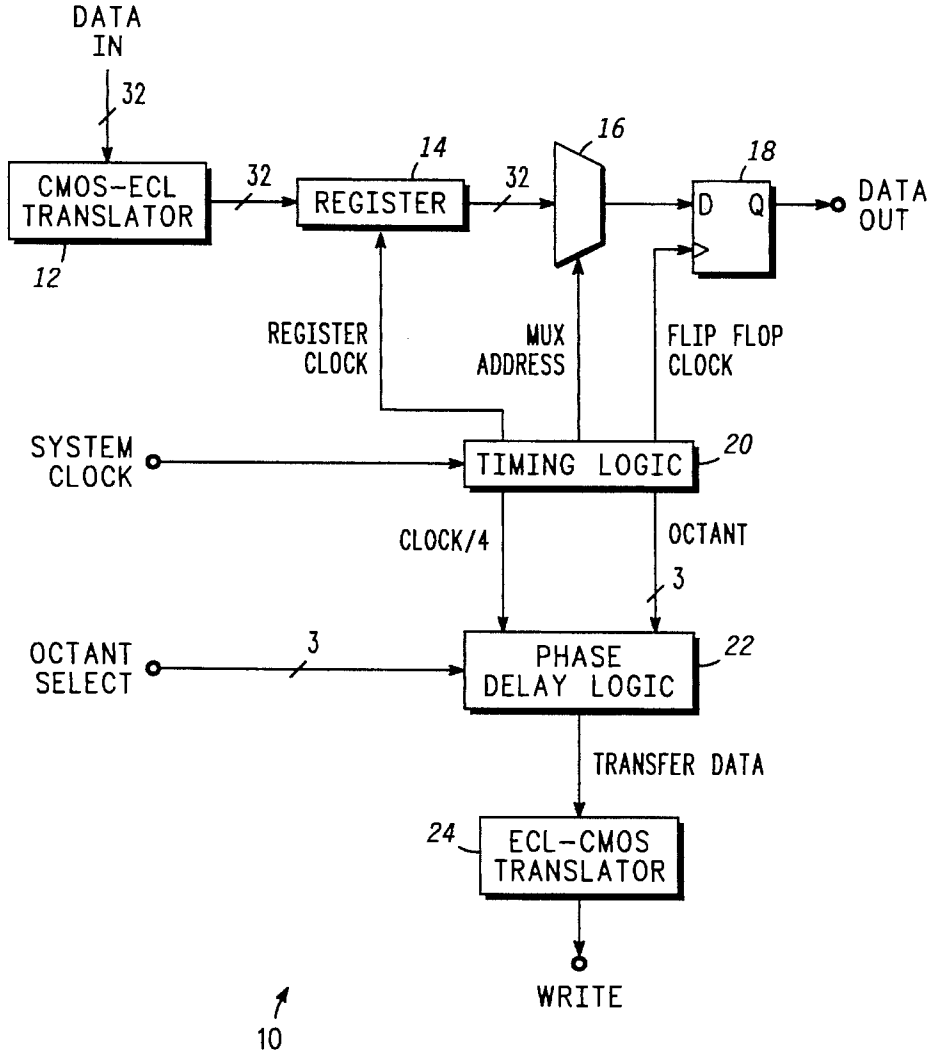
*Primary Examiner*—Marc S. Hoff
*Attorney, Agent, or Firm*—Robert D. Atkins

[57] **ABSTRACT**

A data conversion circuit receives input data from external sourcing logic and performs a parallel-serial conversion. Likewise, a data conversion circuit performs a serial-parallel conversion and presents output data to external sinking logic. In the parallel-serial conversion (**10**), the input data is translated (**12**) and stored in a register (**14**). A multiplexer (**16**) rotates through the data to provide the serial output. In the serial-parallel conversion (**70**), the input data is sequenced into a multiplexer (**74**) to achieve the parallel data word. The parallel data word is stored in a register (**76**) before presenting it to external logic. Phase delay logic (**22**) sets the delay of a transfer data control signal that requests data be read or written. Once the proper delay is determined by experimentation, the phase delay logic controls the phase of the transfer data control signal to request more data at the correct time, or present more data at the correct time, to allow maximum operating speed for the data converter.

**19 Claims, 3 Drawing Sheets**



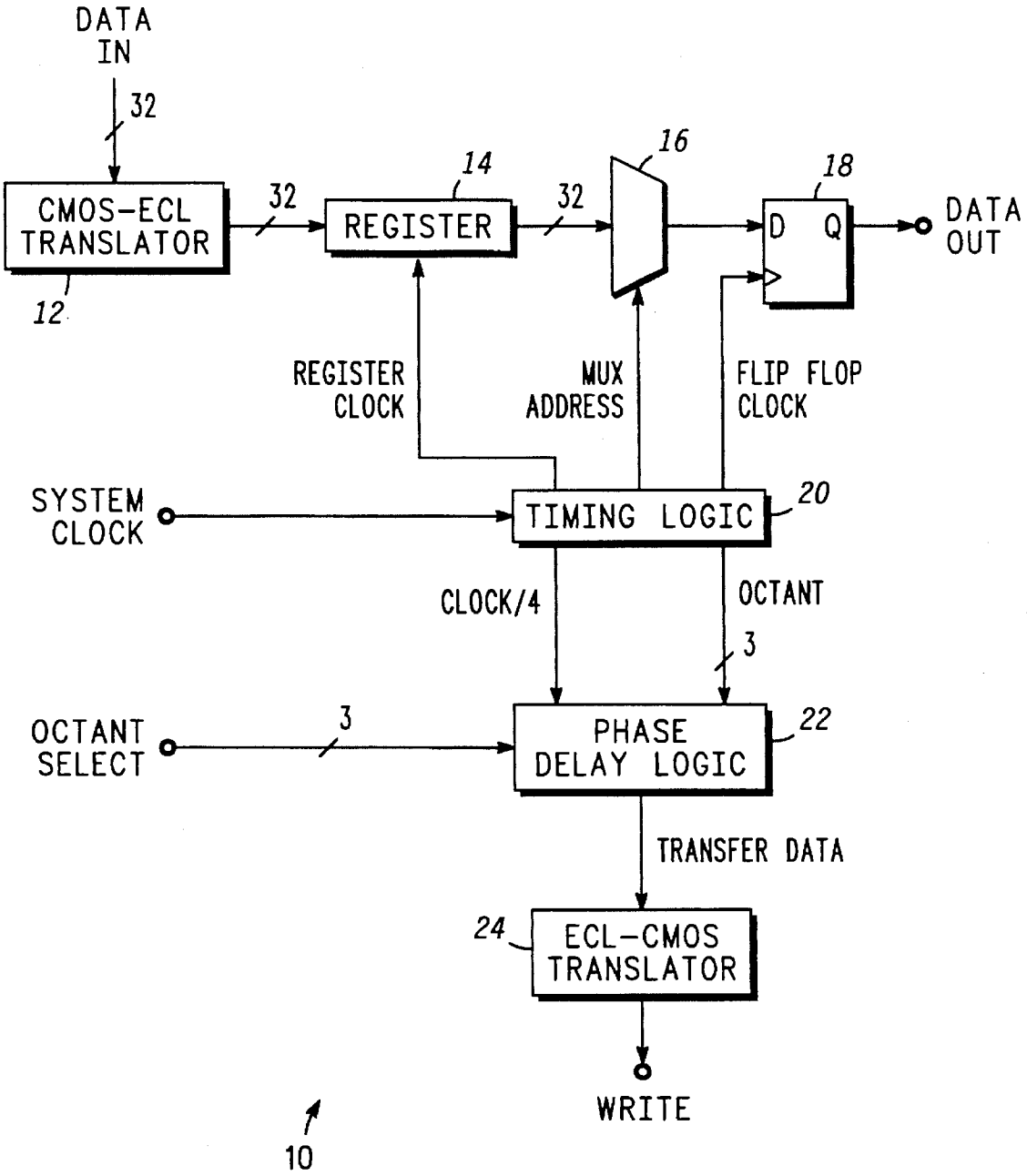

DATA IN
32
CMOS–ECL TRANSLATOR
12
32
REGISTER
14
32
16
18
D Q
DATA OUT
REGISTER CLOCK
MUX ADDRESS
FLIP FLOP CLOCK
SYSTEM CLOCK
TIMING LOGIC
20
CLOCK/4
OCTANT
3
OCTANT SELECT
3
PHASE DELAY LOGIC
22
TRANSFER DATA
24
ECL–CMOS TRANSLATOR
WRITE
10

FIG. 1

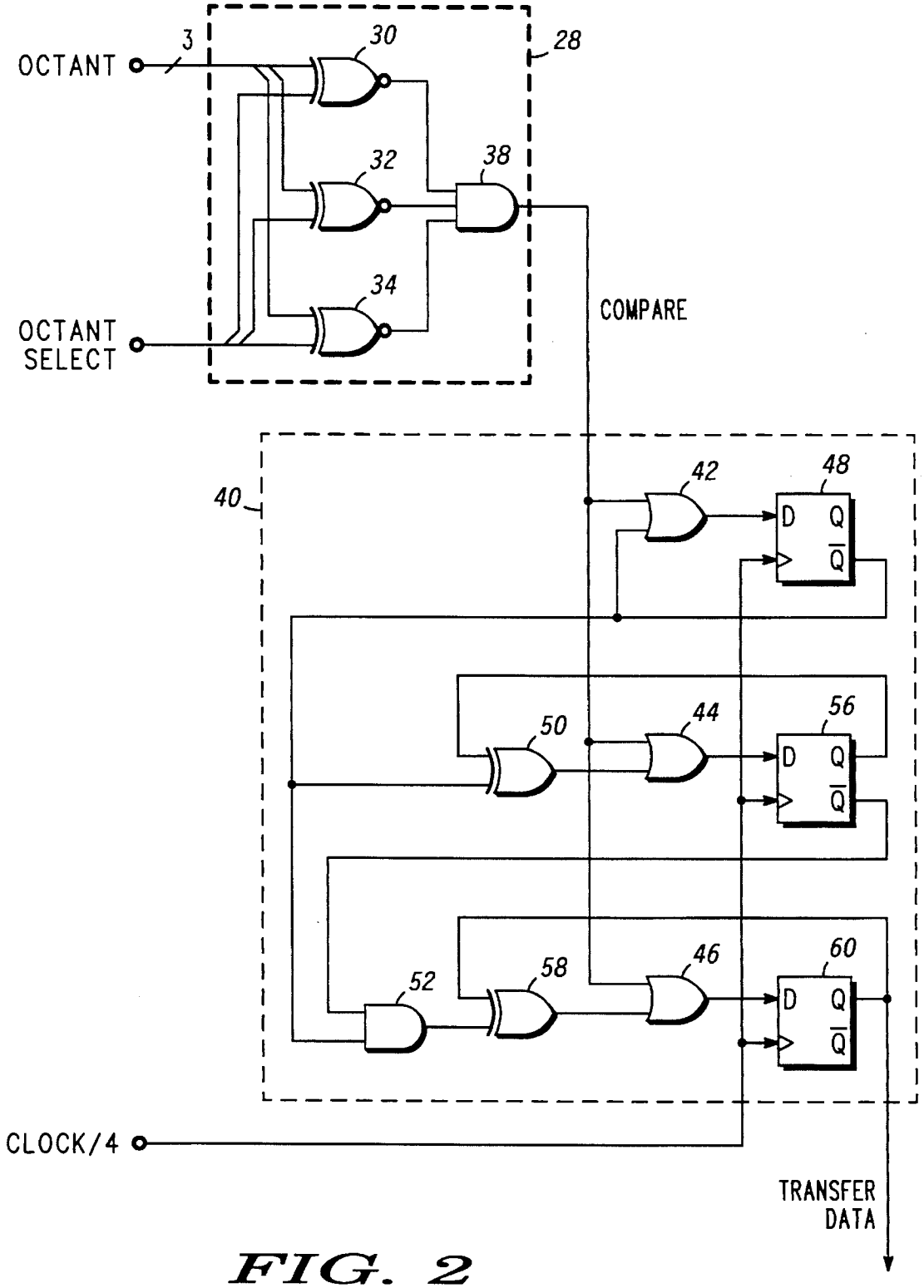

OCTANT
3
30
28
32
38
34
OCTANT SELECT
COMPARE
40
42
48
D
Q
Q
50
44
56
52
58
46
60
CLOCK/4
TRANSFER DATA

FIG. 2

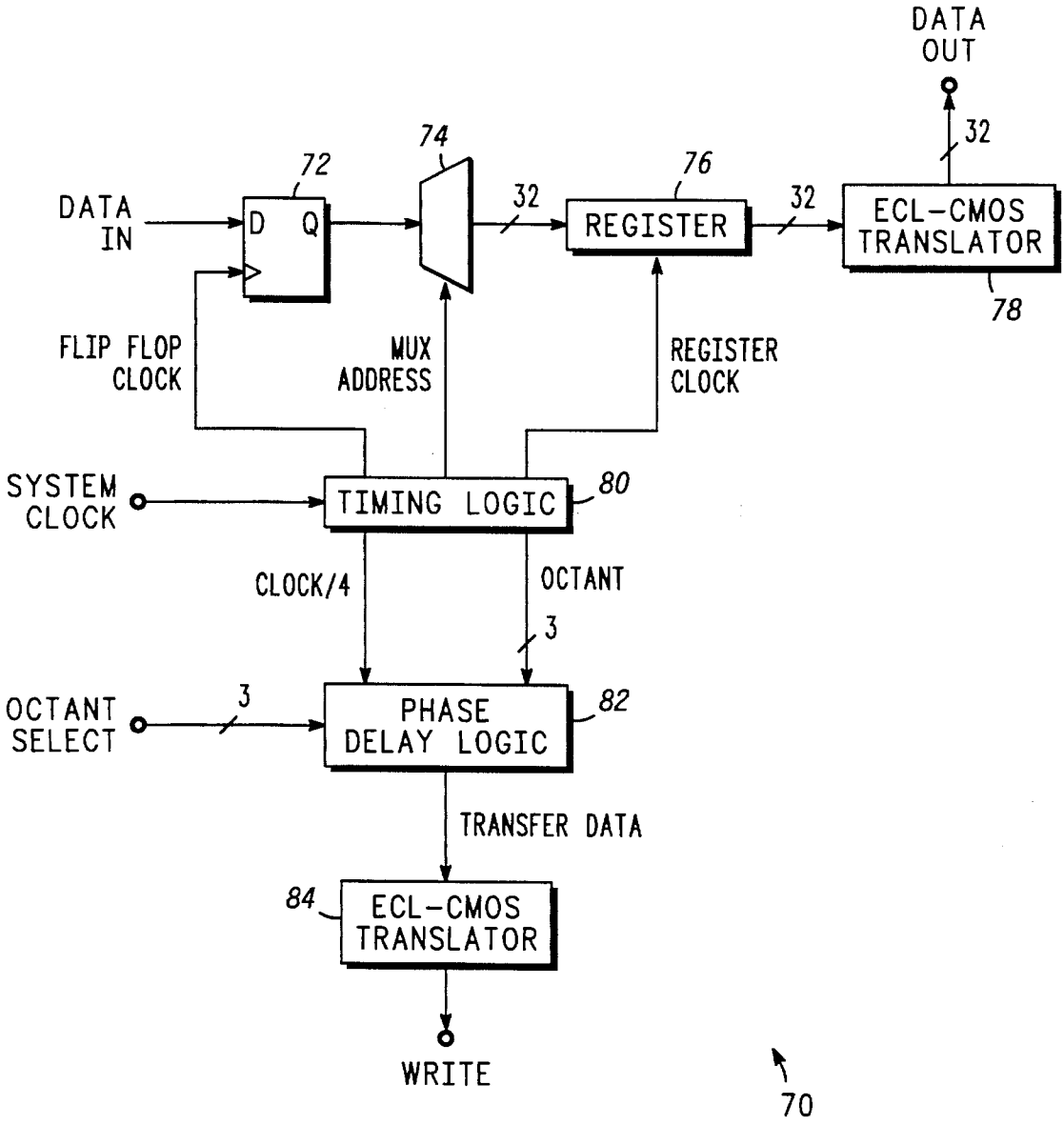

DATA OUT
32
74
72
76
DATA IN
D Q
32
REGISTER
32
ECL-CMOS TRANSLATOR
78
FLIP FLOP CLOCK
MUX ADDRESS
REGISTER CLOCK
SYSTEM CLOCK
TIMING LOGIC
80
CLOCK/4
OCTANT
3
OCTANT SELECT
3
PHASE DELAY LOGIC
82
TRANSFER DATA
84
ECL-CMOS TRANSLATOR
WRITE
70

FIG. 3

# CIRCUIT AND METHOD OF TIMING DATA TRANSFERS

## BACKGROUND OF THE INVENTION

The present invention relates in general to digital timing circuits and, more particularly, to controlling the phase of a data transfer signal to set the proper timing for reading or writing to a data register.

Parallel-serial converters are commonly used in digital circuit design to convert multi-bit signals to a string of data bits that are serially transmitted one at a time. Serial-parallel converters in turn convert the string of data bits back to multi-bit signals. In both applications, a data register is typically embedded within an integrated circuit that periodically receives new data sourced by external logic, or sources new data for external logic. Timing generation logic for reading or writing the data register is also embedded within the integrated circuit. The timing generation logic asserts a periodic signal to the external logic requesting data be presented to or removed from the data register.

Many applications involve high speed operation, say in the gigahertz range. The data transaction must be completed within a predetermined time period. That is, write data must be present and valid for a setup time before, and hold time after it is loaded into the register by a clock signal. Likewise, read data must be present and valid for a setup time before, and hold time after it is read by external logic. Unfortunately at such high data rates, the propagation delay uncertainties of the external logic are almost as long as the entire transaction period.

When the periodic signal is asserted to the external logic, requesting that new data be read or written, the external logic begins the time-consuming process of retrieving or storing new data. In the case of a request from the IC to the external logic to write new data, when the external logic finally presents new data to the integrated circuit, the new data typically propagates through buffer logic and eventually reaches the data register. The internal timing generation logic asserts a clock signal to load the data register. When the data transaction is so fast that propagation delay uncertainties consume almost the entire time period, there is no assurance that data arrives at the data register within register setup and hold-time constraints.

Since the write data register and timing logic are embedded within the integrated circuit, it is difficult to directly measure the actual write setup and hold-time. That is, the setup and hold-time are not readily observable by the external logic. If the write data setup and hold-time are unknown, the data rate of the external sourcing logic must be reduced to ensure sufficient setup and hold-time. Otherwise, where the propagation time uncertainty consumes a large portion of the transaction time period, the data transaction may fail to correctly time the data transfer under a worst-case timing analysis.

Hence, a need exists to properly set the timing of requesting more write data or read data for the data register to achieve maximum data transfer.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram illustrating a parallel-serial converter;

FIG. **2** is a schematic diagram illustrating the phase delay logic of FIG. **1**; and



FIG. **3** is a block diagram illustrating a serial-parallel converter.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIG. **1**, a parallel-serial converter **10** is shown suitable for manufacturing as an integrated circuit using conventional integrated circuit processes. A CMOS-ECL voltage translator circuit **12** receives a 32-bit DATA IN word from external sourcing logic (not shown) operating at CMOS logic levels. CMOS-ECL voltage translator circuit **12** provides a 32-bit signal operating at ECL logic levels to 32-bit register **14**. Register **14** loads data at rising edge of a REGISTER CLOCK signal. Multiplexer **16** rotates through the individual bit locations of register **14** under control of the MUX ADDRESS signal and provides serial bits to the data input of flipflop **18**. Flipflop **18** transfers the serial data signal to DATA OUT at its Q-output upon receiving a FLIPFLOP CLOCK signal.

Timing logic **20** operates in response to a SYSTEM CLOCK signal, running for example at 2.5 gigahertz, for providing the FLIPFLOP CLOCK signal and the REGISTER CLOCK signal. The FLIPFLOP CLOCK signal operates in phase and at the same frequency as the SYSTEM CLOCK. The REGISTER CLOCK signal is derived from dividing the SYSTEM CLOCK by value thirty-two. The REGISTER CLOCK signal is aligned on the same rising edge as the SYSTEM CLOCK. The MUX ADDRESS is reset to zero with each REGISTER CLOCK and counts up with the SYSTEM CLOCK to value thirty-two. Thus, the serialized data stream DATA OUT is sent at the SYSTEM CLOCK frequency with the duration of each serial bit time the same as the period of the SYSTEM CLOCK.

Timing logic **20** further provides a CLOCK/4 signal and a 3-bit OCTANT signal. The CLOCK/4 signal is derived by dividing the SYSTEM CLOCK by value four with alignment on the rising edges of SYSTEM CLOCK. The OCTANT signal takes one of eight binary encoded values (0 through 7) as seen in Table 1. During a first group of four consecutive SYSTEM CLOCKS C0–C3, OCTANT has a value "000". During the second group of four consecutive SYSTEM CLOCKS C4–C7, OCTANT has a value "001", and so on. The OCTANT signal changes state at each rising edge of CLOCK/4, for example, by incrementing a counter (not shown). Timing logic **20** includes combinational logic to divide the SYSTEM CLOCK and reset the MUX ADDRESS signal. Such combinational logic can be implemented from the aforedescribed operations.

TABLE 1

| SYSTEM CLOCK | OCTANT |
|---|---|
| C0–C3 | "000" |
| C4–C7 | "001" |
| C8–C11 | "010" |
| C12–C15 | "011" |
| C16–C19 | "100" |
| C20–C23 | "101" |
| C24–C27 | "110" |
| C28–C31 | "111" |

Phase delay logic circuit **22** receives CLOCK/4 and OCTANT signals from timing logic **20**, and an OCTANT SELECT signal from the external logic (not shown). ECL-CMOS translator **24** converts the TRANSFER DATA signal from phase delay logic circuit **22** to CMOS logic levels for the external logic. Upon receiving the WRITE control

signal, the external logic sends the next 32-bit DATA IN word.

It is important for the overall circuit operation that the output signal from REGISTER **14** does not become metastable. The 32-bit data at the output of translator circuit **12** must be stable for a finite "setup time" before the rising edge of REGISTER CLOCK. Likewise, the 32-bit data must remain stable for a finite "hold-time" after the rising edge of REGISTER CLOCK to ensure that register **14** clocks in valid data. Any violation of setup and hold-time may cause the register output to become metastable, yielding indeterminate logic levels for an indeterminate time duration.

Accordingly, as a feature of the present invention, phase delay logic circuit **22** sets the timing of TRANSFER DATA signal by altering its phase as programmed by the 3-bit OCTANT SELECT signal to request more data at the proper time to allow parallel-serial converter **10** to complete processing the previous data. In practice during a calibration sequence, the OCTANT SELECT signal may be set to various values to determine proper delay time necessary before the WRITE is asserted so that the next DATA IN word arrives at the optimum time to ensure proper data set-up and hold times at the input of register **14** and to allow time to complete processing the previous data. Once the proper delay is determined by experimentation, phase delay logic circuit **22** asserts the TRANSFER DATA signal at the correct time by controlling its phase to allow maximum operating speed for parallel-serial converter **10** given the required set-up and hold-time of register **14**.

Turning to FIG. **2**, further detail of phase delay logic circuit **22** is shown including a digital comparator **28** implemented as exclusive-NOR (XNOR) gates **30**, **32** and **34** and AND gate **38**. XNOR gate **30** receives bit**0** of the OCTANT signal and bit**0** of the OCTANT SELECT signal. XNOR gate **32** receives bit**1** of the OCTANT signal and bit**1** of the OCTANT SELECT signal. XNOR gate **34** receives bit**2** of the OCTANT signal and bit**2** of the OCTANT SELECT signal. The outputs of XNOR gates **32–36** are coupled to inputs of AND gate **38**. If the OCTANT signal matches the OCTANT SELECT signal, AND gate **38** receives all logic ones and provides a logic one COMPARE signal. Otherwise, the COMPARE signal from AND gate **38** is logic zero.

Logic block **40** provides a symmetric 50% duty cycle for the TRANSFER DATA signal by counting down after the COMPARE signal sets the TRANSFER DATA (most significant bit of three bit down-counter) to logic one. The COMPARE signal from AND gate **38** is applied to first inputs of OR gates **42**, **44** and **46**. The output of OR gate **42** is coupled to the D-input of flipflop **48**. The $\overline{Q}$-output of flipflop **48** is coupled to the second input of OR gate **42**, to an input of exclusive-OR (XOR) gate **50**, and to an input of AND gate **52**. The output of XOR gate **50** is coupled to a second input of OR gate **44** that in turn has an output coupled to the D-input of flipflop **56**. The Q-output of flipflop **56** is coupled to the second input of XOR gate **50**, while the $\overline{Q}$-output of flipflop **56** is coupled to the second input of AND gate **52**. The output of AND gate **52** is coupled to a first input of XOR gate **58** that in turn has an output coupled to the second input of OR gate **46**. The output of OR gate **46** is coupled to the D-input of flipflop **60**. The Q-output of flipflop **60** is coupled to the second input of XOR gate **58** and further provides the TRANSFER DATA signal to ECL-CMOS translator **24** in FIG. **1**. Flipflops **48**, **56** and **60** receive the CLOCK/**4** signal at their clock inputs.

During the 32-bit parallel to serial conversion, the 3-bit OCTANT signal increments on every rising edge of CLOCK/**4**, i.e. every four SYSTEM CLOCKS. When the 3-bit OCTANT signal matches the externally-supplied 3-bit OCTANT SELECT signal, the COMPARE signal is asserted as logic one. The Q-outputs of flipflops **48**, **56** and **60** go to logic one on the next rising edge of the CLOCK/**4** signal. The TRANSFER DATA signal goes to logic one. When the OCTANT signal increments to its next value and COMPARE returns to logic zero, flipflops **48**, **56** and **60** operate as a 3-bit synchronous down counter and decrement with each rising edge of CLOCK/**4**. Since the TRANSFER DATA signal is the most significant bit of the down counter, it remains logic one for the first half of the counts and returns to logic zero for the second half of the counts. Logic block **40** thus provides a symmetric 50% duty cycle for the TRANSFER DATA signal.

For example, assume that the 32-bit DATA IN signal is latched into register **14** by the REGISTER CLOCK. In the present example, it has been determined by experimentation that the OCTANT SELECT signal "001" sets the proper phase delay before asserting TRANSFER DATA to the external logic to send the next DATA IN word. The delay determines the amount of time parallel-serial converter **10** needs to complete processing the present data word and be ready for the next. Assume that the Q-outputs of the flipflops begin at logic one and the $\overline{Q}$-outputs begin as logic zero. The first four SYSTEM CLOCKS C**0**–C**3** correspond to multiplexer **16** reading the four least significant bits D**0**–D**3** from register **14**. At the first rising edge of CLOCK/**4** (clock C**0**), the OCTANT signal is "**000**" and does not match the OCTANT SELECT signal "001". Consequently, the COMPARE signal is logic zero.

At the second rising edge of CLOCK/**4** (clock C**4**), the OCTANT signal switches to "001" and matches the OCTANT SELECT signal causing the COMPARE signal goes to logic one. The outputs of OR gates **42–46** go to logic one due to the logic one COMPARE signal for the initial state of the down count. Four SYSTEM CLOCKS later, the third rising edge of CLOCK/**4** (clock C**8**) clocks the logic ones into flipflops **48**, **56** and **60** and sets their Q-outputs to logic one. The OCTANT signal switches to "010" and no longer matches the OCTANT SELECT signal. The COMPARE signal returns to logic zero. XOR gate **50** receives a logic zero from the $\overline{Q}$-output of flipflop **48** and a logic one from the Q-output of flipflop **56** and sets the second input of OR gate **44** to logic one. The D-input of flipflop **56** receives a logic one from OR gate **44**. AND gate **52** receives logic zeroes from flipflops **48** and **56**. XOR gate **58** receives a logic zero from AND gate **52** and a logic one from flipflop **60** and provides a logic one to OR gate **46**. The D-input of flipflop **60** goes to logic one.

The fourth rising edge of CLOCK/**4** (clock C**12**) sets the $\overline{Q}$-output of flipflop **48** to logic one while the Q-outputs of flipflops **56** and **60** remain logic one. The output of OR gate **42** goes to logic one. XOR gate **50** receives a logic one from the $\overline{Q}$-output of flipflop **48** and a logic one from the Q-output of flipflop **56** and sets the second input of OR gate **44** to logic zero. The D-input of flipflop **56** receives a logic zero from OR gate **44**. AND gate **52** receives a logic one from flipflop **48** and a logic zero from flipflop **56**. XOR gate **58** receives a logic zero from AND gate **52** and a logic one from flipflop **60** and provides a logic one to OR gate **46**. The D-input of flipflop **60** goes to logic one.

The fifth rising edge of CLOCK/**4** (clock C**16**) sets the Q-outputs of flipflops **48** and **60** to logic one while the Q-output of flipflop **56** goes to logic zero. The output of OR gate **42** goes to logic zero. XOR gate **50** receives logic zeroes from the $\overline{Q}$-output of flipflop **48** and the Q-output of

flipflop **56** and sets the second input of OR gate **44** to logic zero. The D-input of flipflop **56** receives a logic zero from OR gate **44**. AND gate **52** receives a logic zero from flipflop **48** and a logic one from flipflop **56**. XOR gate **58** receives a logic zero from AND gate **52** and a logic one from flipflop **60** and provides a logic one to OR gate **46**. The D-input of flipflop **60** goes to logic one.

The sixth rising edge of CLOCK/4 (clock **C20**) sets the $\overline{Q}$-outputs of flipflops **48** and **56** to logic one while the Q-output of flipflop **60** remains logic one. XOR gate **50** receives a logic one from the $\overline{Q}$-output of flipflop **48** and a logic zero from the Q-output of flipflop **56** and sets the second input of OR gate **44** to logic one. The D-input of flipflop **56** receives a logic one from OR gate **44**. AND gate **52** receives logic ones from flipflops **48** and flipflop **56**. XOR gate **58** receives a logic one from AND gate **52** and a logic one from flipflop **60** and provides a logic zero to OR gate **46**. The D-input of flipflop **60** goes to logic zero.

The seventh rising edge of CLOCK/4 (clock **C24**) sets the TRANSFER DATA signal to logic zero. The TRANSFER DATA signal remains logic zero for the next four CLOCK/4 cycles, i.e. **C24–C31** and **C0–C7**, as the down counter completes the second half of its count down sequence. Logic **40** thus provides a symmetric 50% duty cycle. Either edge of the TRANSFER DATA signal may be used to trigger the external logic to send more data to parallel-serial converter **10**. By controlling the phase of TRANSFER DATA, the correct timing is established for data transfer so that the requested data arrives at the optimum time to maximize the operating speed of parallel-serial converter **10**.

The aforedescribed phase control over the TRANSFER DATA is equally applicable to serial-parallel conversion such as shown in FIG. **3**. Serial-parallel converter **70** is shown suitable for manufacturing as an integrated circuit using conventional integrated circuit processes. The data input of flipflop **72** receives the serial DATA IN signal from external sourcing logic (not shown) and passes it to multiplexer **74** at each FLIPFLOP CLOCK. Multiplexer **74** rotates through its individual bit locations under control of the MUX ADDRESS signal and provides parallel bits to register **76**. Register **76** loads data at rising edge of a REGISTER CLOCK signal. A CMOS-ECL voltage translator circuit **78** converts the 32-bit data word from register **76** to CMOS logic levels.

Timing logic **80** operates in response to a SYSTEM CLOCK signal, operating for example at 2.5 gigahertz, for providing the FLIPFLOP CLOCK signal and the REGISTER CLOCK signal. The FLIPFLOP CLOCK signal operates in phase and at the same frequency as the SYSTEM CLOCK. The REGISTER CLOCK signal are derived from dividing the SYSTEM CLOCK by value thirty-two. The REGISTER CLOCK signal is aligned on the same rising edge as the SYSTEM CLOCK. The MUX ADDRESS is reset to zero with each REGISTER CLOCK and counts up with the SYSTEM CLOCK to value thirty-two. Thus, the serialized data stream DATA OUT is sent at the SYSTEM CLOCK frequency with the duration of each serial bit time the same as the period of the SYSTEM CLOCK. Timing logic **20** further provides a CLOCK/4 signal and a 3-bit OCTANT signal. The CLOCK/4 signal is derived by dividing the SYSTEM CLOCK by value four aligned with the rising edges of SYSTEM CLOCK. The OCTANT signal takes one of eight binary encoded values (0 through 7) as seen in Table 1. Timing logic **80** includes combinational logic to divide the SYSTEM CLOCK and reset the MUX ADDRESS signal. Such combinational logic can be implemented from the aforedescribed operations.

Phase delay logic circuit **82** receives CLOCK/4 and OCTANT signals from timing logic **80**, and an OCTANT SELECT signal from external logic (not shown). ECL-CMOS translator **84** converts the TRANSFER DATA signal from phase delay logic circuit **82** to CMOS logic levels for the external logic. Upon receiving the WRITE control signal, the external logic sends the next DATA IN bit. Phase delay logic circuit **82** follows the same description given in FIG. **2** and asserts the TRANSFER DATA signal at the correct time to allow maximum operating speed for serial-parallel converter **70** given the required set-up and hold-time of register **76**.

By now it should be appreciated that the present invention provides proper timing of the data transfer between external data sourcing or sinking logic and data conversion circuits. Phase delay logic sets the delay for a transfer data control signal as programmed by a select signal. During a calibration sequence, the select signal is set to various values to determine proper delay time necessary before requesting that more data be read or written. Once the proper delay is determined by experimentation, the phase delay logic circuit asserts the transfer data signal at the correct time by controlling its phase, to allow maximum operating speed for the data conversion given the required set-up and hold-time of the embedded register and of the external logic. By controlling the phase of transfer data requests, the correct timing is established to ensure proper data set-up and hold times and to allow complete processing before the next data word needs to be read or written.

While specific embodiments of the present invention have been shown and described, further modifications and improvements will occur to those skilled in the art. It is understood that the invention is not limited to the particular forms shown and it is intended for the appended claims to cover all modifications which do not depart from the spirit and scope of this invention. The present invention is applicable to other types of data processing circuits that must control timing of incoming data.

What is claimed is:

**1**. A phase delay circuit, comprising:

a comparator having first and second inputs and an output, said first input receiving a first control signal, said second input receiving a second control signal, said output providing a compare signal having a first state when said first and second control signals match; and

a down counter responsive to said compare signal for initializing a count value and responsive to a clock signal for counting down to generate an output signal having a symmetric duty cycle.

**2**. The circuit of claim **1** wherein said down counter includes:

a first OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal; and

a first flipflop having a data input, a clock input, and an inverted output, said data input being coupled to said output of said first OR gate, said inverted output being coupled to said second input of said first OR gate, said clock input being coupled for receiving said clock signal.

**3**. The circuit of claim **2** wherein said down counter further includes:

a first exclusive-OR gate having first and second inputs and an output, said first input being coupled to said inverted output of said first flipflop;

a second OR gate having first and second inputs and an output, said first input being coupled for receiving said

compare signal, said second input being coupled to said output of said first exclusive-OR gate; and

a second flipflop having a data input, a clock input, and first and second complementary outputs, said data input being coupled to said output of said second OR gate, said first complementary output being coupled to said second input of said first exclusive-OR gate, said clock input being coupled for receiving said clock signal.

**4**. The circuit of claim **3** wherein said down counter further includes:

a first AND gate having first and second inputs and an output, said first input being coupled to said inverted output of said first flipflop, said second input being coupled to said second complementary output of said second flipflop;

a second exclusive-OR gate having first and second inputs and an output, said first input being coupled to said output of said first AND gate;

a third OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal, said second input being coupled to said output of said second exclusive-OR gate; and

a third flipflop having a data input, a clock input, and an output, said data input being coupled to said output of said third OR gate, said output being coupled to said second input of said second exclusive-OR gate and providing said output signal of said down counter, said clock input being coupled for receiving said clock signal.

**5**. The circuit of claim **4** wherein said comparator includes:

a third exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a first bit of said first control signal, said second input being coupled for receiving a first bit of said second control signal;

a fourth exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a second bit of said first control signal, said second input being coupled for receiving a second bit of said second control signal; and

a second AND gate having first and second inputs and an output, said first input being coupled to said output of said third exclusive-OR gate, said second input being coupled to said output of said fourth exclusive-OR gate, said output providing said compare signal.

**6**. The circuit of claim **5** wherein said comparator further includes a fifth exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a third bit of said first control signal, said second input being coupled for receiving a third bit of said second control signal, said output being coupled to a third input of said second AND gate.

**7**. A method of selecting phase delay of a transfer data control signal, comprising the steps of:

comparing first and second control signals and generating a compare signal having a first state when said first and second control signals match; and

initializing a count value in response to said compare signal; and

counting down said count value in response to a clock signal to provide a most significant bit of said count value with a symmetric duty cycle.

**8**. A data conversion circuit, comprising:

a register having an input coupled for receiving parallel input data and having an output;

a multiplexer having an input coupled to said output of said register for providing serial data;

a comparator having first and second inputs and an output, said first input receiving a first control signal, said second input receiving a second control signal, said output providing a compare signal having a first state when said first and second control signals match; and

a down counter responsive to said compare signal for initializing a count value and responsive to a clock signal for counting down to generate a transfer data signal having a symmetric duty cycle to enable transfer of said parallel input data to said register.

**9**. The circuit of claim **8** wherein said down counter includes:

a first OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal; and

a first flipflop having a data input, a clock input, and an inverted output, said data input being coupled to said output of said first OR gate, said inverted output being coupled to said second input of said first OR gate, said clock input being coupled for receiving said clock signal.

**10**. The circuit of claim **9** wherein said down counter further includes:

a first exclusive-OR gate having first and second inputs and an output, said first input being coupled to said inverted output of said first flipflop;

a second OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal, said second input being coupled to said output of said first exclusive-OR gate; and

a second flipflop having a data input, a clock input, and first and second complementary outputs, said data input being coupled to said output of said second OR gate, said first complementary output being coupled to said second input of said first exclusive-OR gate, said clock input being coupled for receiving said clock signal.

**11**. The circuit of claim **10** wherein said down counter further includes:

a first AND gate having first and second inputs and an output, said first input being coupled to said inverted output of said first flipflop, said second input being coupled to said second complementary output of said second flipflop;

a second exclusive-OR gate having first and second inputs and an output, said first input being coupled to said output of said first AND gate;

a third OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal, said second input being coupled to said output of said second exclusive-OR gate; and

a third flipflop having a data input, a clock input, and an output, said data input being coupled to said output of said third OR gate, said output being coupled to said second input of said second exclusive-OR gate and providing said output signal of said down counter, said clock input being coupled for receiving said clock signal.

**12**. The circuit of claim **11** wherein said comparator includes:

a third exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a first bit of said first control signal, said second input being coupled for receiving a first bit of said second control signal;

a fourth exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a second bit of said first control signal, said second input being coupled for receiving a second bit of said second control signal; and

a second AND gate having first and second inputs and an output, said first input being coupled to said output of said third exclusive-OR gate, said second input being coupled to said output of said fourth exclusive-OR gate, said output providing said compare signal.

**13**. The circuit of claim **12** wherein said comparator further includes a fifth exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a third bit of said first control signal, said second input being coupled for receiving a third bit of said second control signal, said output being coupled to a third input of said second AND gate.

**14**. A data conversion circuit, comprising:

a multiplexer having an input coupled for receiving serial input data and having an output;

a register having an input coupled to said output of said register for providing prarllel data;

a comparator having first and second inputs and an output, said first input receiving a first control signal, said second input receiving a second control signal, said output providing a compare signal having a first state when said first and second control signals match; and

a down counter responsive to said compare signal for initializing a count value and responsive to a clock signal having a symmetric duty cycle to enable transfer of said serial input data to said register.

**15**. The circuit of claim **14** wherein said down counter includes:

a first OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal; and

a first flipflop having a data input, a clock input, and an inverted output, said data input being coupled to said output of said first OR gate, said inverted output being coupled to said second input of said first OR gate, said clock input being coupled for receiving said clock signal.

**16**. The circuit of claim **15** wherein said down counter further includes:

a first exclusive-OR gate having first and second inputs and an output, said first input being coupled to said inverted output of said first flipflop;

a second OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal, said second input being coupled to said output of said first exclusive-OR gate; and

a second flipflop having a data input, a clock input, and first and second complementary outputs, said data input being coupled to said output of said second OR gate, said first complementary output being coupled to said second input of said first exclusive-OR gate, said clock input being coupled for receiving said clock signal.

**17**. The circuit of claim **161**wherein said down counter further includes:

a first AND gate having first and second inputs and an output, said first input being coupled to said inverted output of said first flipflop, said second input being coupled to said second complementary output of said second flipflop;

a second exclusive-OR gate having first and second inputs and an output, said first input being coupled to said output of said first AND gate;

a third OR gate having first and second inputs and an output, said first input being coupled for receiving said compare signal, said second input being coupled to said output of said second exclusive-OR gate; and

a third flipflop having a data input, a clock input, and an output, said data input being coupled to said output of said third OR gate, said output being coupled to said second input of said second exclusive-OR gate and providing said output signal of said down counter, said clock input being coupled for receiving said clock signal.

**18**. The circuit of claim **17** wherein said comparator includes:

a third exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a first bit of said first control signal, said second input being coupled for receiving a first bit of said second control signal;

a fourth exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a second bit of said first control signal, said second input being coupled for receiving a second bit of said second control signal; and

a second AND gate having first and second inputs and an output, said first input being coupled to said output of said third exclusive-OR gate, said second input being coupled to said output of said fourth exclusive-OR gate, said output providing said compare signal.

**19**. The circuit of claim **18** wherein said comparator further includes a fifth exclusive-OR gate having first and second inputs and an output, said first input being coupled for receiving a third bit of said first control signal, said second input being coupled for receiving a third bit of said second control signal, said output being coupled to a third input of said second AND gate.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

# CERTIFICATE OF CORRECTION

PATENT NO. : 5,563,594
DATED : October 8, 1996
INVENTOR(S) : David K. Ford et al.

It is certified that error appears in the above-indentified patent and that said Letters Patent is hereby corrected as shown below:

In claim 14, column 9, line 30, insert --for counting down to generate a transfer data signal-- after "signal".

In claim 17, column 10, line 7, delete "161wherein" and insert --16 wherein--.

Signed and Sealed this

Twenty-ninth Day of April, 1997

*Attest:*

*Attesting Officer*

BRUCE LEHMAN

*Commissioner of Patents and Trademarks*

# EXHIBIT D

# United States Patent [19]

**Schuster et al.**

[11] **Patent Number: 5,000,827**

[45] **Date of Patent: Mar. 19, 1991**


[54] **METHOD AND APPARATUS FOR ADJUSTING PLATING SOLUTION FLOW CHARACTERISTICS AT SUBSTRATE CATHODE PERIPHERY TO MINIMIZE EDGE EFFECT**


[75] Inventors: **Virgil E. Schuster; Reginald K. Asher, Sr.,** both of Scottsdale; **Bhagubhai D. Patel,** Tempe, all of Ariz.

[73] Assignee: **Motorola, Inc.,** Schaumburg, Ill.



[21] Appl. No.: **459,892**

[22] Filed: **Jan. 2, 1990**

[51] **Int. Cl.**[5] ..... **C25D 5/02**

[52] **U.S. Cl.** ..... **204/15**

[58] **Field of Search** ..... 204/15



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198017 8/1989 Japan .
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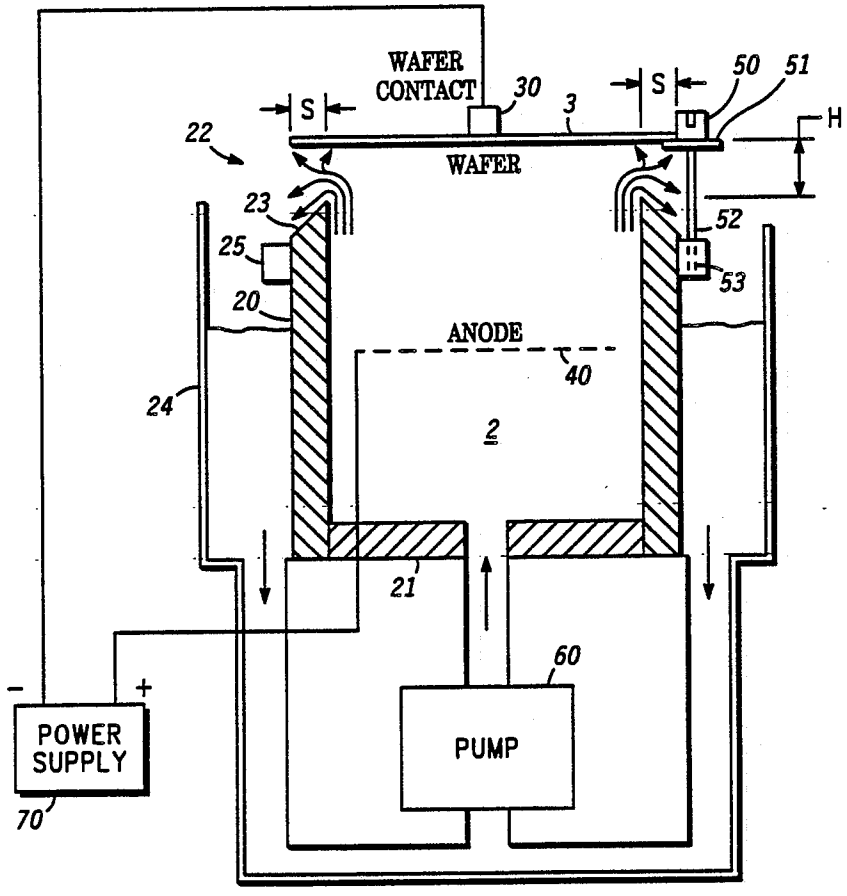
*Primary Examiner*—T. M. Tufariello
*Attorney, Agent, or Firm*—Charles R. Lewis; Walter W. Nielsen



[57] **ABSTRACT**

A method and apparatus for electroplating metallized bumps of substantially uniform height on predetermined terminal areas of a substrate. Cup plating apparatus includes elements for adjusting parameters affecting the geometry of the substrate relative to the plating cup, as well as flow rate of the electroplating solution against the substrate surface. By achieving non-laminar flow of the electroplating solution near the substrate edges, the plating characteristics of the electroplating solution are altered in this region, substantialy offsetting "edge effect", so that the resulting plated bump height is substantially uniform across the substrate.


**2 Claims, 7 Drawing Sheets**



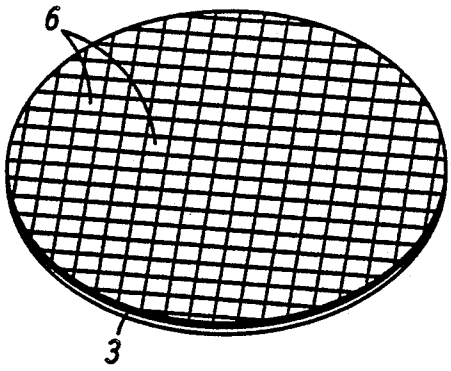



FIG. 1

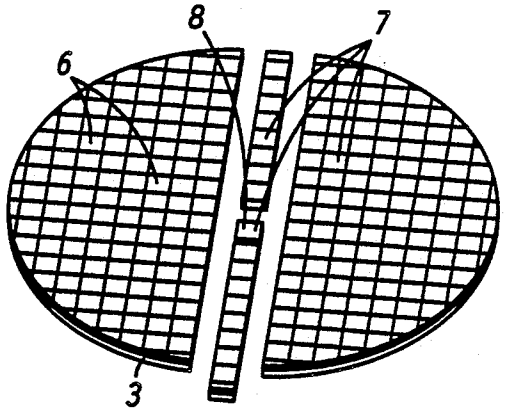



FIG. 2

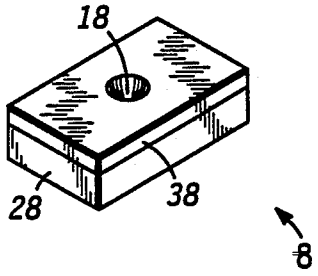



FIG. 3A

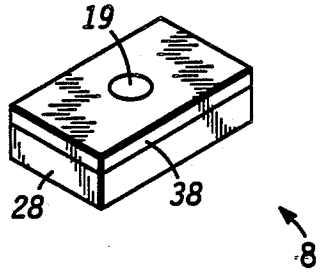



FIG. 3B

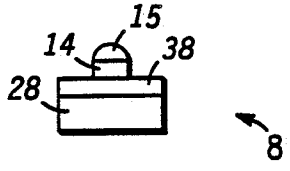



FIG. 3C

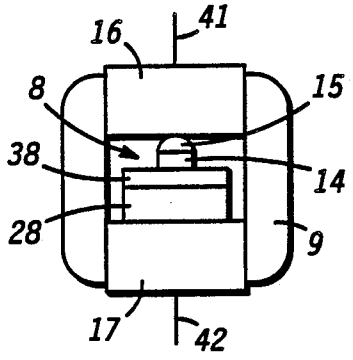



FIG. 4

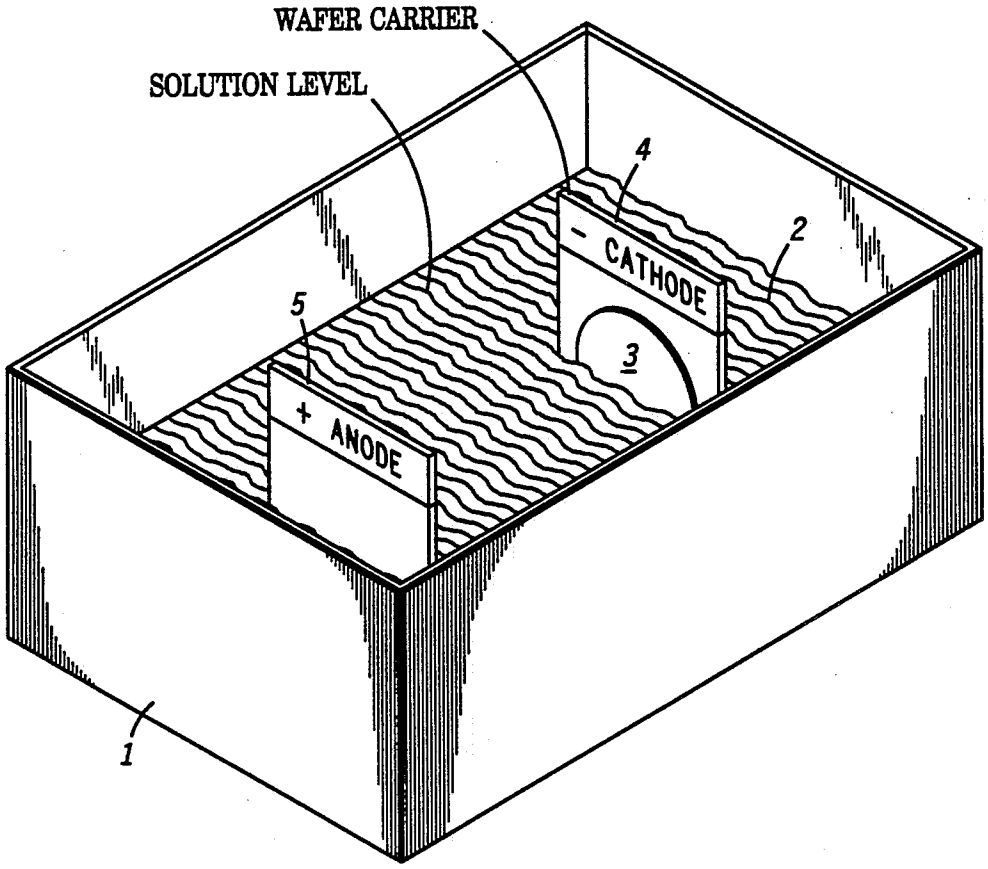
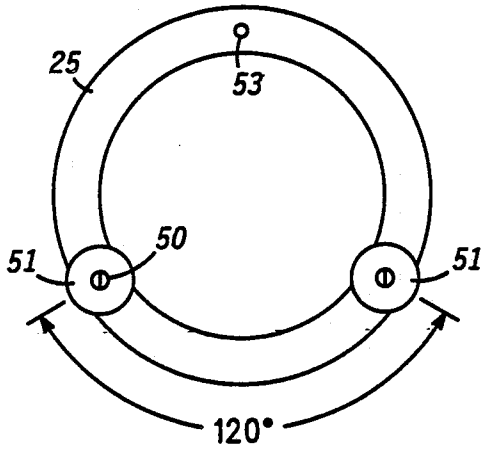
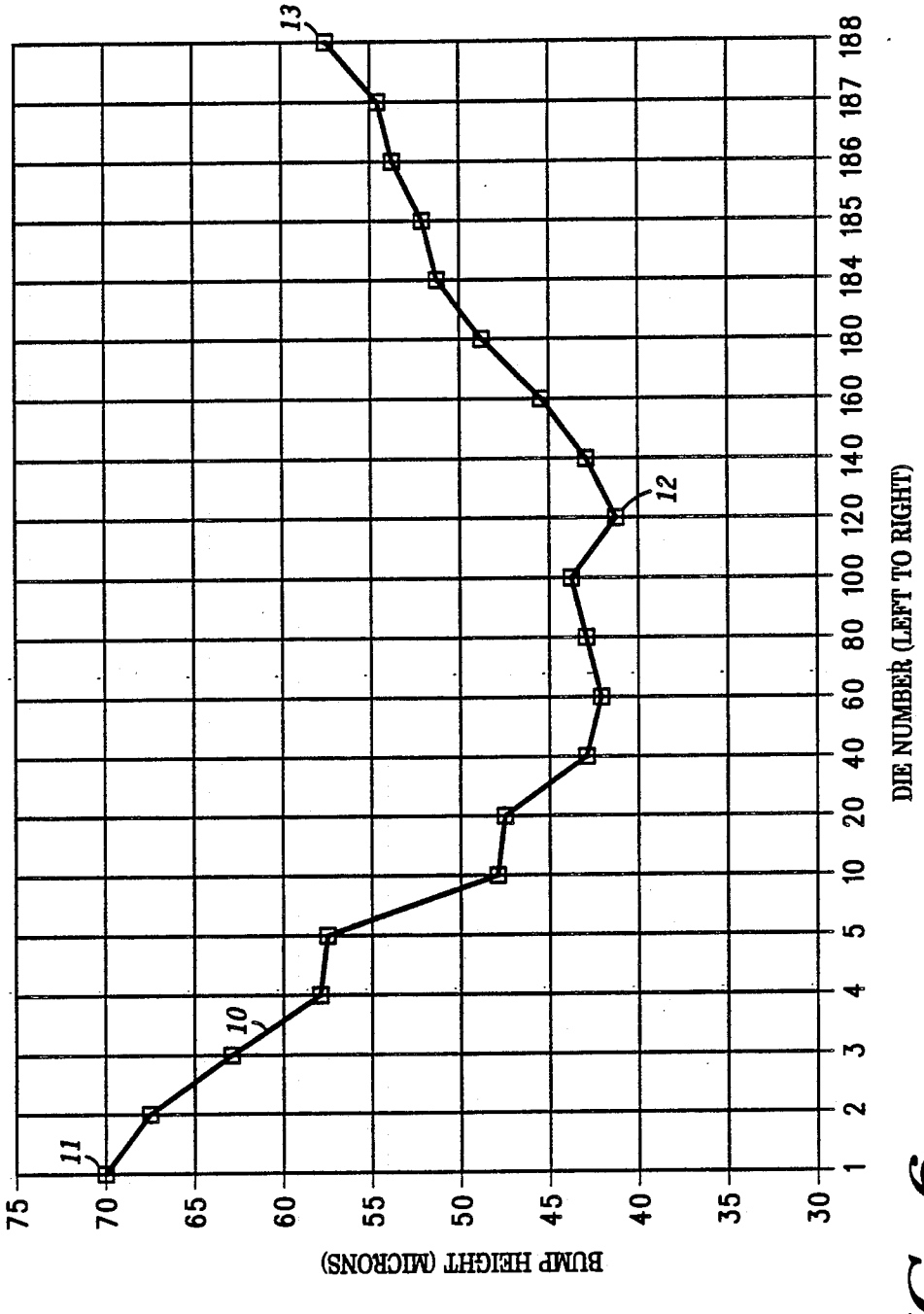



FIG. 5
-PRIOR ART-

FIG. 8

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DIE NUMBER (LEFT TO RIGHT)

FIG. 6

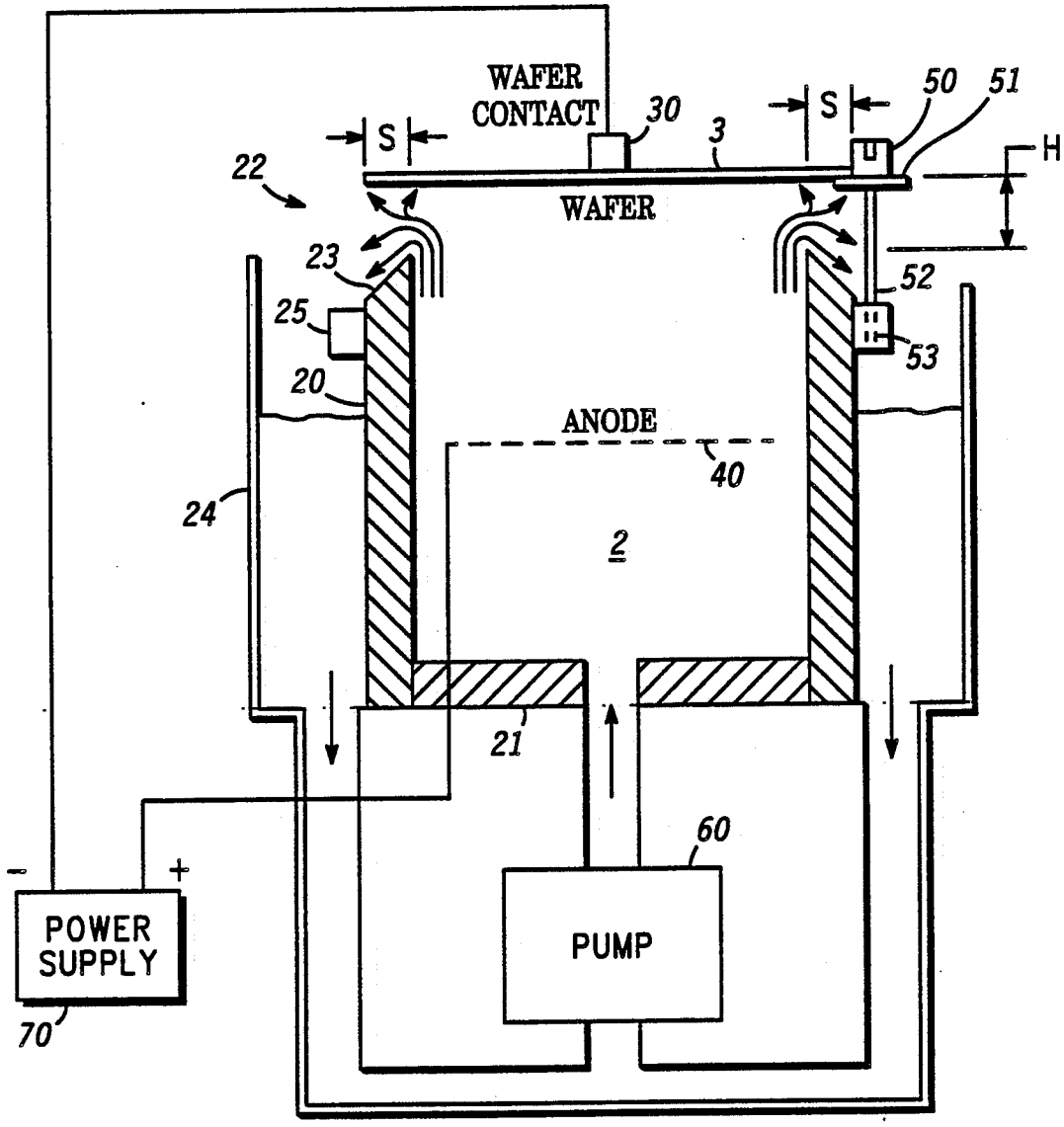
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FIG. 7

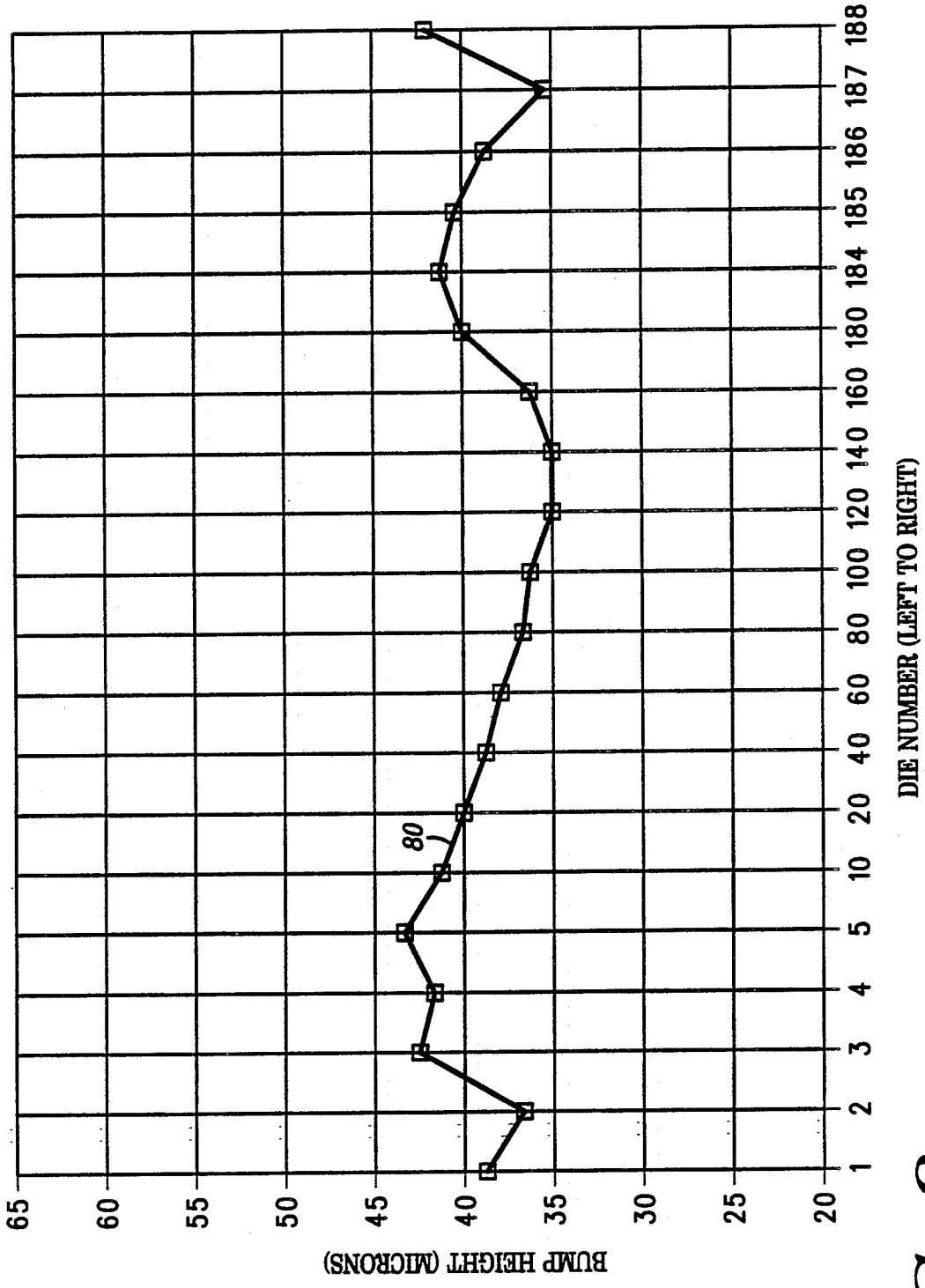
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FIG. 9

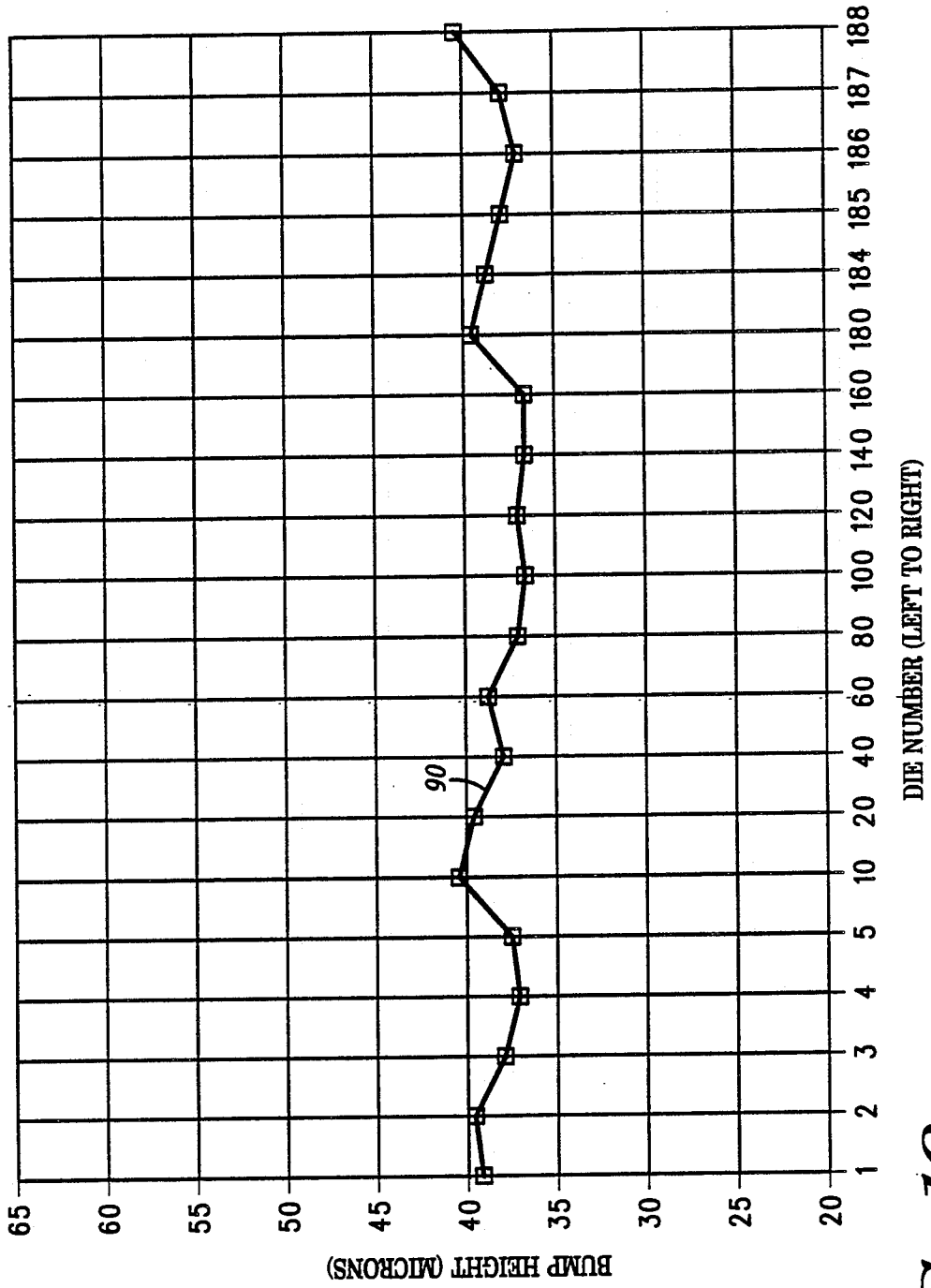
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FIG. 10

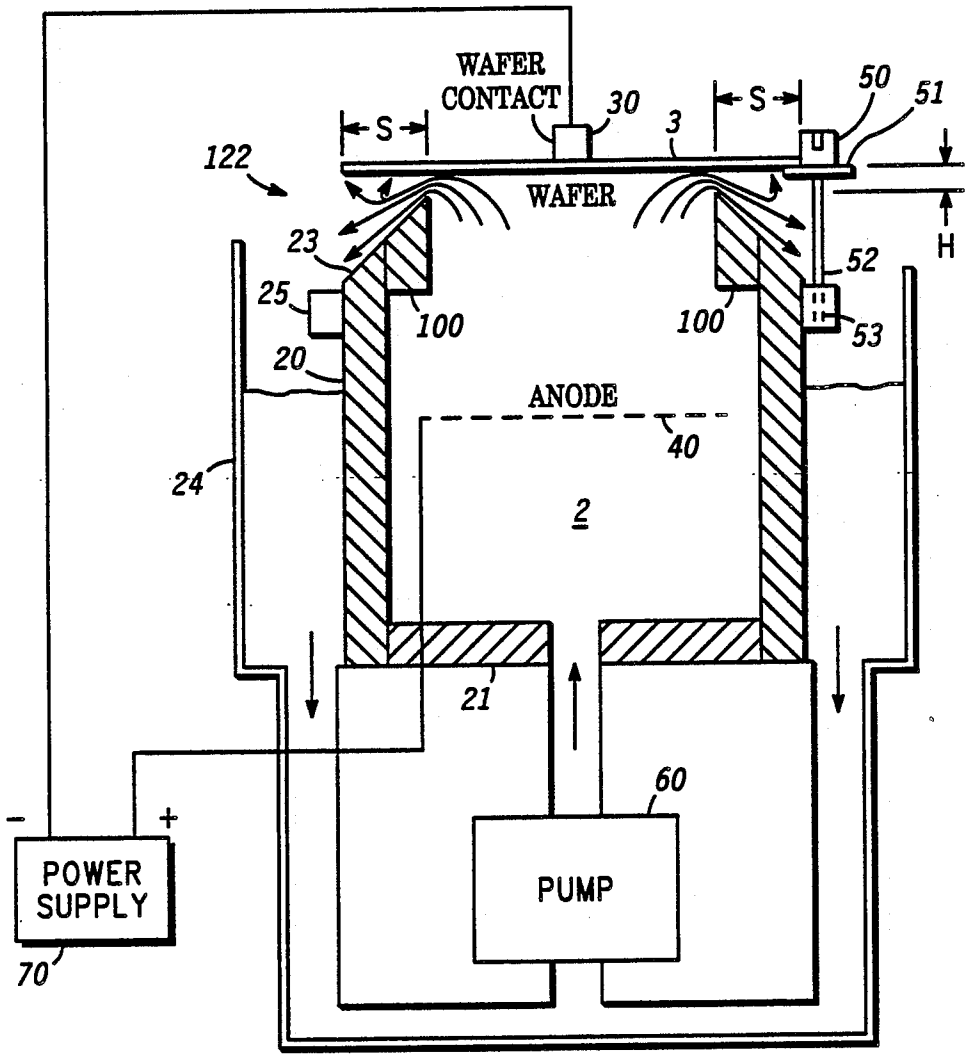
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FIG. 11

# METHOD AND APPARATUS FOR ADJUSTING PLATING SOLUTION FLOW CHARACTERISTICS AT SUBSTRATE CATHODE PERIPHERY TO MINIMIZE EDGE EFFECT

## BACKGROUND OF THE INVENTION

1. Technical Field of the Invention

This invention relates generally to the manufacture of micro-electrical circuits, and, more particularly, to the formation of uniform-thickness metallization bumps on terminal areas of electrical circuits on a substantially planar substrate, particularly near the edge thereof.

2. Background Information

The present invention has utility in the plating of metallization bumps on predetermined terminal areas of silicon wafers prior to scribing such wafers into a plurality of individual die.

FIG. 1 shows a silicon wafer 3 upon which a plurality of individual electrical circuit elements 6 are formed. The electrical characteristics of individual circuit elements 6 may be imparted to them by employing any suitable process(es) therefor. The specifics of the electrical circuit of the circuit elements 6 lies outside of the scope of the present invention.

FIG. 2 shows a view similar to that shown in FIG. 1, wherein the wafer 3 has been separated into pieces 7 including at least one die 8 using conventional wafer scribing or sawing techniques.

FIGS. 3A show steps in the formation of a terminal region 19 on a surface of an individual die 8, prior to wafer scribing or sawing, and the plating of a metallization bump onto such terminal region 19. In the manufacture of a particular electrical product from die 8, such as the double-slug diode shown in FIG. 4, it is frequently necessary to deposit a metallized bump in a predetermined area of a surface of such die.

Referring to FIG. 3A, a representative individual die 8 of wafer 3 is shown overlaid with a layer of oxide 38, and a hole or window 18 has been etched through the oxide 38 down to a terminal area (not shown) of the underlying substrate 28.

In FIG. 3B, the window 18 of FIG. 3A has been filled with top metal 19. In a preferred embodiment of the invention, the top metal 19 actually comprises three layers: first a layer of titanium, next a layer of nickel, and finally a layer of silver. Again, the composition of the layers and thickness thereof are not specific to the present invention.

In FIG. 3C, a metallization bump, comprising a layer of silver 14 and a layer of tin 15, has been electro-deposited over the top metal terminal region 19.

FIG. 4 shows a double-slug diode manufactured according to the method and apparatus disclosed by the present invention. The diode of FIG. 4 is shown for illustrative purposes only, and it should be understood by all practitioners in the art that the present invention has broad utility in many metallization bump processing applications and is not intended to be limited to implementations such as that shown in FIGS. 3 and 4.

Still with reference to FIG. 4, the die 8 has been separated from its counterparts on wafer 3 and mounted between copper "slugs" or terminals 16 and 17 to which electrical leads 41 and 42, respectively, have been affixed. The entire assembly is enclosed in glass 9.

FIG. 5 shows a prior art plating apparatus for plating metallization bumps onto predetermined terminal areas of a silicon wafer, such as terminal area 19 of die 8.



Referred to as a rack plating apparatus, it comprises a tank 1 of electroplating solution into which an anode 5 and a cathode 4 are shown partially submersed. It will be understood that anode 5 and cathode 4 are shown partially submersed for ease in understanding and that during operation they are substantially submersed.

Anode 5 has a potential having a positive polarity coupled thereto, while cathode 4 has a potential having a negative polarity coupled thereto.

Affixed to cathode 4 is a substantially planar, conductive wafer 3 comprising a plurality of individual electrical elements (not shown), each with a terminal area such as terminal area 19 shown in FIG. 3B. It will be understood by those skilled in the art that substrate 3 may itself serve as the cathode 4, or substrate 3 may be suitably affixed to a wafer carrier, which serves as the cathode 4.

FIG. 6 is a graph illustrating the variation of bump height across a silicon wafer electroplated with the prior art plating apparatus shown in FIG. 5. The bump height in microns measured on selected die is provided along the Y-axis, and the die position across a given wafer diameter is provided along the X-axis. It will be observed that the X-axis of FIG. 6 is non-linerar, in that emphasis is given to die numbers closest to the wafer edge, for example die numbers 1–5 at the left edge and die number 184–188 at the right edge.

It is seen that when metallized bumps are plated with the apparatus shown in FIG. 6 there is substantial variation in bump height across the wafer diameter. The bumps are highest at or near the wafer edge. For example, the bump height 11 of die #1 is 70 microns, and that of die #188 is approximately 58 microns, whereas that of die #120 is approximately 41 microns.

According to the graph of FIG. 6, the bump height variation across a typical 9.65 centimeter diameter wafer is almost 30 microns, ranging from a minimum of 41 microns at die #120 to a maximum of 70 microns at die #1. This greatly exceeds a desired production specification width of 20 microns.

The increased electroplating intensity near the wafer edge is commonly referred to as "edge effect".

Therefore, there is a substantial need to provide an electroplating method and apparatus which overcomes the "edge effect" problem known in prior electroplating systems.

Various electroplating systems are known which have attempted to overcome the "edge effect". One such system is referred to as a cathode-mask system, in which the high-growth area of the substrate is masked. However, this system suffers from the need to achieve critcal positioning of the mask relative to the high-growth area of the substrate. Both the alignment of the mask and the mask-to-wafer spacing are critical and difficult to control.

## BRIEF SUMMARY OF INVENTION

The present invention solves the problem of "edge effect" by selectively altering the metallic ion concentration of the electroplating solution near the edge(s) of the wafer substrate.

According to the present invention, the electroplating solution is contained in a cup-shaped container. A pump circulates the solution through an inlet and out over the lip of the cup. The wafer is suspended at an optimum height above the cup lip. The cup diameter is optimized relative to the wafer diameter and to the area

in which undue bump growth occurs. In addition, the flow rate of solution through the plating cup is optimized. By optimizing the above-mentioned parameters, the metallic ion concentration of the electroplating solution in the vicinity of the wafer edge(s) is optimized to just offset the "edge effect", and to provide substantially uniform height of electroplated bumps across the wafer diameter.

Accordingly, it is an object of the present invention to provide an electroplating method and apparatus which produce metallized bumps of substantially uniform height across a substrate including the edge(s) thereof.

Thus a greater proportion of die fall within desired specifications, resulting in lower rejection rates, lower material and labor charges, higher quality, and greater customer acceptance.

It is another object of the present invention to provide an electroplating method and apparatus which is relatively inexpensive and which is relatively easy to control.

It is yet another object of the present invention to provide an electroplating method and apparatus which eliminates the labor-intensive steps of mounting a substrate on a wafer carrier prior to electrodepositing the metallized bumps, demounting the substrate from the wafer carrier after deposition, and cleaning the mounting agent (typically wax, glycol, or plastic) from the substrate.

These and other objects are achieved in accordance with a preferred embodiment of the invention by providing a method of forming metallization bumps on predetermined terminal areas of a planar substrate, the bumps being of substantially uniform height across the substrate, wherein the method comprises (a) providing a planar substrate having thereon a multiplicity of terminal areas; (b) applying an electrical potential having a first electrical polarity to the terminal areas; (c) applying an electrical potential having a second electrical polarity to an electrical terminal immersed in a container of an electroplating solution; (d) exposing the substrate to the electroplating solution to permit the growth of the metallization bumps on the terminal areas: and (e) controlling the growth of the metallization bumps in a predetermined region of the substrate by altering the metallic ion concentration of the electroplating solution in the predetermined region.

## BRIEF DESCRIPTION OF THE DRAWINGS

The invention is pointed out with particularity in the appended claims. However, other features of the invention will become more apparent and the invention will be best understood by referring to the following detailed description in conjunction with the accompanying drawings in which:

FIG. 1 shows a silicon wafer upon which a plurality of individual electrical circuit elements are formed.

FIG. 2 shows a view similar to that shown in FIG. 1, wherein the wafer has been separated into pieces including at least one die.

FIGS. 3A, 3B and 3C show steps in the plating of a metallization bump onto a terminal area of an individual die.

FIG. 4 shows a double-slug diode manufactured according to the method and apparatus disclosed by the present invention.

FIG. 5 shows a prior art plating apparatus for plating metallization bumps onto predetermined terminal areas of a silicon wafer.

FIG. 6 is a graph illustrating the variation of bump height across a silicon wafer electroplated with the prior art plating apparatus shown in FIG. 5.

FIG. 7 shows a cross-sectional view of apparatus for plating metallization bumps of substantially uniform height onto predetermined terminal areas of a silicon wafer, according to the present invention.

FIG. 8 shows a top-view of ring element 25 and adjustable wafer support elements 51 of the plating apparatus shown in FIG. 7.

FIG. 9 is a graph illustrating the variation of bump height across a silicon wafer electroplated according to the method of the present invention.

FIG. 10 is another graph illustrating the variation of bump height across a silicon wafer electroplated according to the method of the present invention.

FIG. 11 shows a cross-sectional view of an alternative embodiment of apparatus for plating metallizaton bumps of substantially uniform height onto predetermined terminal areas of a silicon wafer, according to the present invention.

## DESCRIPTION OF PREFERRRED EMBODIMENT

FIG. 7 shows apparatus for plating metallization bumps of substantially uniform height onto predetermined terminal areas of a silicon wafer, according to the present invention. A cylcindrical cup 20 of suitable material, such as polyvinylchloride (PVC) or polypropylene, contains the desired electroplating solution, which in a preferred embodiment is a cyanide silver plating solution. The bottom portion of cup 20 may be formed integrally therewith or may be formed separately, as shown by bottom portion 21.

Pump 60 circulates the plating solution 2 through an inlet in the bottom cup 20, and plating solution 2 exists cup 20 over the lip 23 into tank or sump 24, from which it is eventually returned to the inlet side of pump 60.

To a suitable power supply 70, such as a pulsing DC rectifier, are coupled a wafer contact 30 and an anode 40. Anode 40 may take the form of a platinum-clad tantalum screen immersed in the electroplating solution. Wafer contact 30 may take the form of a silver-clad nickel element which rests upon or is affixed to the upper surface of water or substrate 3. Wafer 3 functions as a cathode.

Wafer 3 is supported by several wafer support members 51 suitably mounted in a ring or collar member 25 around the periphery of cup 20 (refer to FIG. 8). Support member 25 may take the form of a PVC washer mounted on a PVC screw 52, having a slotted head 50, and being threaded into a mating opening 53 in ring 25.

FIG. 8 shows a top-view of ring element 25 and adjustable wafer support elements 51 of the plating apparatus shown in FIG. 7. In a preferred embodiment, three wafer support elements 51 are spaced substantially equidistantly around the periphery of ring 25, and each has a slotted head to facilitate adjusting the height of wafer 3 above the lip 23 of cup 20.

### Operation of Preferred Embodiment

In operation, as mentioned above, electroplating solution 2 flows generally upwards from the inlet in the bottom of cup 20, against the underside of wafer 3, and out over the lip 23 into sump 24.

Cup plating apparatus is known in the art and, as used, suffers from the well-known "edge effect". However, according to the present invention the metallic ion concentration of electroplating solution **2** is altered in the region near the edge of wafer **3**, so as to effectively offset the "edge effect".

By creating non-laminar flow of the electroplating solution **2** through the opening between the lip **23** and lower surface of wafer **3**, the plating characteristics of solution **2** near the edge are altered from those elsewhere within cup **20**. The plating effect of the solution is weakened, thereby offsetting the tendency for increased plating effect near the cathode edge. The precise reasons as to why turbulent flow of the electroplating solution **2** against the outer portions of wafer **3** causes an offsetting of the "edge effect" are not completely understood.

To produce the non-laminar flow over the optimum peripheral area of wafer **3**, the distance S between the outer edge of wafer **3** and the inner surface of cup **20** should be optimized. The parameter S is changed by changing the diameter of cup **20** relative to the diameter of wafer **3**. By decreasing the diameter, a relatively greater peripheral area of wafer **3** is affected by a slight reduction in bump growth rate, whereas increasing the diameter of cup **20** diminishes the peripheral area of wafer **3** which is affected. In a preferred embodiment of the invention, the diameter of the wafer was 9.65 centimeters, and the inside diameter of the cup was 8.89 centimeters.

Another important dimension which should be optimized is the distance H between the lower surface of wafer **3** and the top of cup lip **23**. If H is too low, laminar flow apparently results, and there is relatively little offsetting of the "edge effect", resulting in relatively higher bumps near the edge. As H is increased, turbulent flow apparently results, perhaps due to the capillary attraction of the bottom surface of wafer **3** near the edge, and there is increased offsetting of the "edge effect", resulting in edge bumps which are nearly identical in height to bumps elsewhere across the wafer diameter (refer to FIG. **10**).

Flow rate through the plating cup **20** was found not to be a critical parameter. In a preferred embodiment, a flow rate of 4 to 5 liters/minute was employed.

The invention described herein was used successfully to plate bumps comprising an initial layer of silver and a subsequent layer of tin, resulting in metallization bumps substantially as depicted in FIG. **3C**.

FIG. **9** is a graph illustrating the variation of bump height across a silicon wafer electroplated according to the method of the present invention. To produce the results illustrated in FIG. **9**, the height H of wafer **3** above the lip **23** of cup **20** was set at 2.25 millimeters. This produced a bump height variation across the wafer ranging from a high of 43 microns to a low of 35 microns (i.e. with a process variation of approximately 8 microns), which is well within a desired specification width of 20 microns.

FIG. **10** is another graph illustrating the variation of bump height across a silicon wafer electroplated according to the method of the present invention. By raising the height H of wafer **3** above the lip **23** of cup **20** to 2.45 millimeters, the bump height variation across the wafer ranged from a high of 40 microns to a low of 36 microns (i.e. with a process variation of approximately 4 microns). This is a substantial improvement over the process variation of 30 microns produced by the known tank electroplating method.

## Description of Alternative Embodiment

FIG. **11** shows an alternative embodiment of apparatus for plating metallization bumps of substantially uniform height onto predetermined terminal areas of a silicon wafer, according to the present invention.

The apparatus illustrated in FIG. **11** differs from that shown in FIG. **7** only in that the distance S between the outer edge of wafer **3** and the inner surface of cup **20** has been increased through the use of an annular ring **100** suitably secured within the lip portion **23** of cup **20**. This is shown merely as one example of how the distance S may be altered.

It will be apparent to those skilled in the art that the disclosed invention may be modified in numerous ways and may assume many embodiments other than the preferred form specifically set out and described above.

For example, the present invention can be extended to electroplating of ceramic substrates. It may also be extended to electroplating metals other than those mentioned herein. The plating cup may take the form of a pipe or other suitable geometric shape.

Accordingly, it is intended by the appended claims to cover all modifications of the invention which fall within the true spirit and scope of the invention.

What is claimed is:

**1**. A method of forming metallized bumps on predetermined terminal areas of a planar substrate, said bumps being of substantially uniform height across said substrate, wherein said method comprises:

(a) providing a planar substrate having thereon a multiplicity of terminal areas;

(b) applying an electrical potential having a first electrical polarity to said terminal areas;

(c) applying an electrical potential having a second electrical polarity to an electrical terminal immersed in a container of an electroplating solution;

(d) exposing said substrate to said electroplating solution to permit the growth of said metallization bumps on said terminal areas;

(e) controlling the growth of said metallization bumps in a predetermined region of said substrate by altering the metallic ion concentration of said electroplating solution in said predetermined region;

(f) providing said container with an opening whose shape approximates that of said substrate;

(g) positioning said substrate proximate to said container opening;

(h) providing an inlet within said container for pumping said solution into said container, said solution exiting said container through said opening;

wherein said metallic ion concentration of said electroplating solution is changed by:

(i) in step (f) altering the size of said opening;

(j) in step (g) altering the distance of said substrate from said container opening; and

(k) in step (h) altering the flow rate of said solution through said opening.

**2**. The method of according to claim **1**, wherein said metallization bumps comprise metal selected from the group consisting of silver and tin.

* * * * *

# EXHIBIT E

US005252177A

# United States Patent [19]

Hong et al.

[11] Patent Number: 5,252,177

[45] Date of Patent: Oct. 12, 1993

[54] METHOD FOR FORMING A MULTILAYER WIRING OF A SEMICONDUCTOR DEVICE

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[73] Assignee: **SamSung Electronics Co., Ltd.**, Suwon, Rep. of Korea

[21] Appl. No.: **736,772**

[22] Filed: **Jul. 29, 1991**

[30] **Foreign Application Priority Data**

Apr. 15, 1991 [KR] Rep. of Korea ..... 1991-6024

[51] **Int. Cl.**[5] ..... **B44C 1/22**; C23F 7/00

[52] **U.S. Cl.** ..... **156/643**; 156/644; 156/657; 156/656; 156/667; 204/192.32; 437/228; 437/235

[58] **Field of Search** ..... 156/643, 644, 651, 652, 156/655, 656, 657, 659.1, 662, 667; 204/192.32, 192.35; 437/180, 187, 198, 199, 203, 228, 235, 238

[56] **References Cited**

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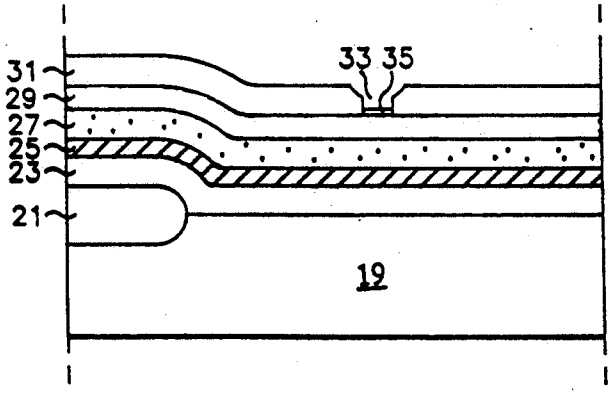
*Primary Examiner*—William A. Powell

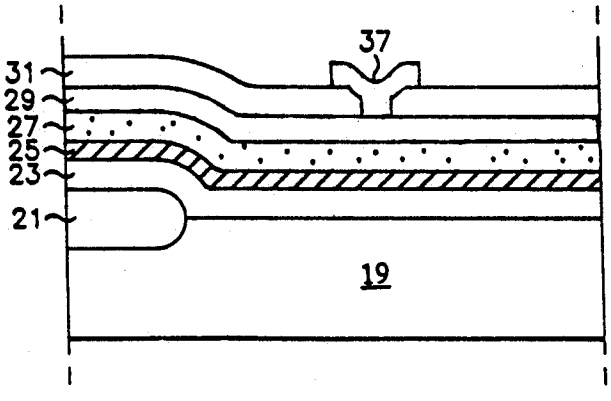
*Attorney, Agent, or Firm*—Robert E. Bushnell

[57] **ABSTRACT**

A method for forming a multilayer wiring, in a method for manufacturing a semiconductor device, is disclosed. The method comprises: forming a contact hole **33** on the surface of a conductive layer **29** by a photolithography, removing a photoresist by using plasma ashing at a predetermined temperature, pressure and amount of oxygen per unit cubic, and simultaneously forming a protective layer **35** consisting of a oxide layer on the surface of the exposed conductive layer. Thus, damage of the surface of wiring caused by the chemical reaction of an organic solvent and water in the subsequent process thereof, is prevented, to provide high density and high speed semiconductor integrated circuit whose electrode characteristics between two wiring layers is improved.

**15 Claims, 2 Drawing Sheets**



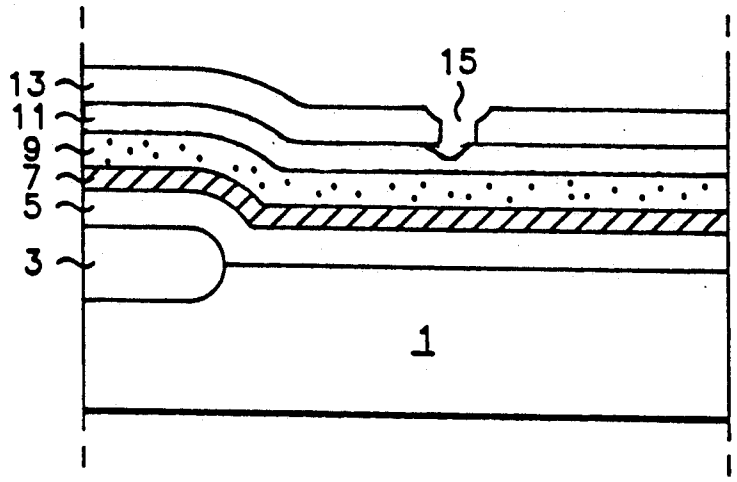



Fig. 1A
(Prior Art)

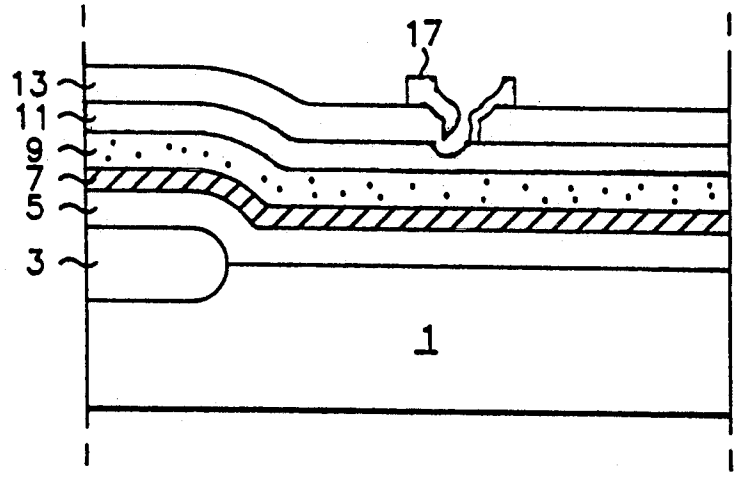



Fig.1B
(Prior Art)

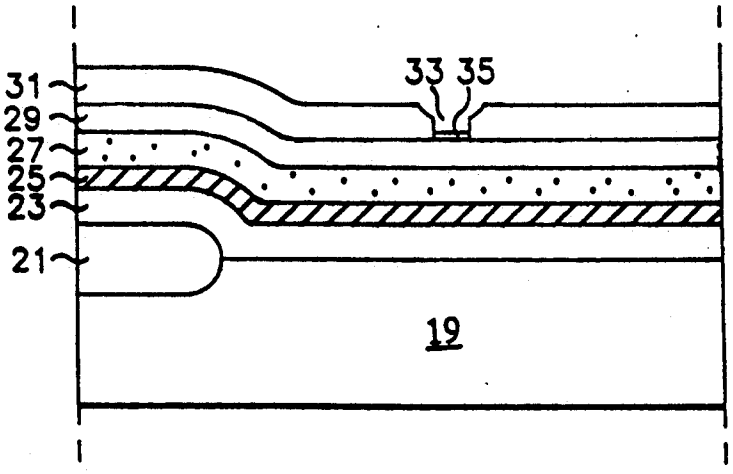



FIG. 2A

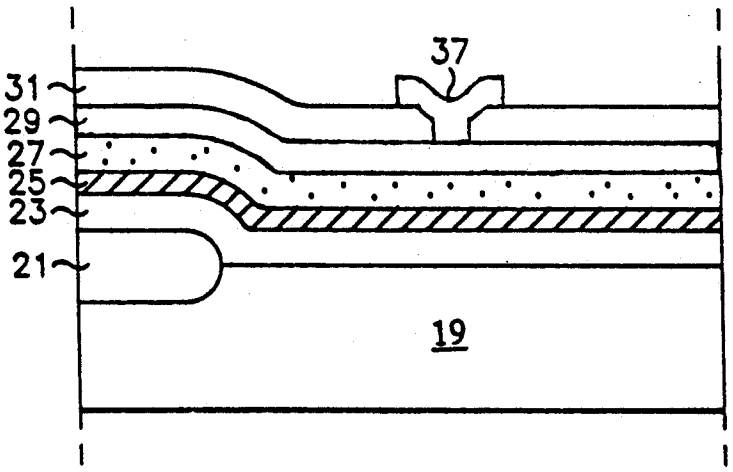



FIG. 2B

# METHOD FOR FORMING A MULTILAYER WIRING OF A SEMICONDUCTOR DEVICE

## FIELD OF THE INVENTION

The present invention relates to a method for manufacturing a semiconductor device, and more particularly to a method for forming multilayer wiring.

## BACKGROUND OF THE INVENTION

Recently, the density of semiconductor devices and operating speeds thereof have been increased. However, in case of a semiconductor integrated circuit having conventional one layer wiring, a reduction in the width of metal wiring in the memory device increased electrical resistance. Thus, the power consumption increases. Accordingly, to enhance operating speed, multilayer wiring has been proposed. A material metal wiring is aluminum containing silicon of under 4% to prevent aluminum spike occurred when forming wiring with pure aluminum. However, aluminum wiring containing added copper added has been proposed to improve reliability.

FIGS. 1A and 1B illustrate a conventional method for manufacturing a semiconductor device having multilayer wiring. In the FIG. 1A, on a semiconductor substrate 1 of a first conductivity type, where field oxide layer 3 for isolation is formed, a first insulation layer 5, a first conductive layer 7, a second insulation layer 9, a second conductive layer **11** and a third insulation layer 13 are consecutively deposited. Then, a contact hole 15 is formed through selective etching of the third insulation layer 13 by photolithography. Thus, the top surface of the second conductive layer 11 is partially exposed. Here, the first conductive layer 7 is bit line, and the second conductive layer 11 is aluminum wiring containing silicon of about 1% and copper of about 0.5%. By employing the above mentioned aluminum in the metal wiring, hillock and electromigration characteristics can be improved as compared with conventional aluminum wiring containing only silicon. The wiring made of the second conductive layer 11 and another wiring (not shown) are contacted through the contact hole 15. In forming the described wiring of multilayer structure, in practice, underlying layer wiring can be damaged by the chemical reaction of copper component extracted into the grain boundary of the aluminum, water ($H_2O$) and organic solvents, etc, which occur during removal of the ordinary photoresist. That is, to expose the surface of the underlying layer wiring, plasma ashing (process of developing a photoresist and thereafter removing the photoresist remaining after plasma etching process), dipping in an organic solvent such that sulfate acid, rinsing with water and drying are progressively carried out to remove the remaining photoresist positioned on the upper surface of the insulation layer. At this time, the exposed portions of aluminum wiring containing copper directly contact the organic solvent and water. As a result, the copper component existing in grain boundary of the aluminum is discolored with black spots and pieces of the second conductive layer **11** may drop away. The size of these pieces can be 1$\mu$m in diameter. The resultant damage of the wiring is shown in the FIG. **1A**. When an overlying layer wiring is formed by the vapor deposition and the underlying layer wiring is damaged, step coverage is inferior. Accordingly the overlying layer wiring is shorted or the contact area is decreased



increasing contact resistance. Thus electrical characteristic of devices deteriorates.

FIG. **1B** illustrates the cross sectional view of the conventional multilayer wiring. On the third conductive layer of aluminum, an overlying layer wiring **17** is disposed by formation of a pattern and selective etching. As shown in FIG. **1B**, a portion of the overlying layer wiring contacting the underlying layer wiring small because of the interior step coverage.

As described above, conventional method has a problem that the wiring is damaged by exposure of the underlying layer wiring through the contact hole, when the remaining photoresist disposed over the underlying layer is removed after forming the contact hole on the underlying layer wiring. Therefore, reliable semiconductor integrated circuit is not obtained.

## SUMMARY OF THE INVENTION

It is an object of the invention to provide a method for forming a multilayer wiring, and preventing damage of exposed wiring upon removing of a photoresist residue.

To achieve the above object, the method includes the steps of: forming a contact hole for contacting an underlying layer wiring and an overlying layer wiring, removing the remaining photoresist positioned on an insulation layer, the insulation layer being disposed on the underlying layer wiring, by plasma ashing under condition of the predetermined temperature, pressure and amount of oxygen per unit cubic, and simultaneously forming an oxide layer on the exposed underlying layer wiring through the contact hole; and, removing the oxide layer just before forming of the overlying layer wiring.

## BRIEF DESCRIPTION OF THE DRAWINGS

The above objects and other advantages of the present invention will become more apparent by describing in detail the preferred embodiment of the present invention with the reference to the attached drawings, in which:

FIGS. **1A** and **1B** are views illustrating conventional manufacturing process; and

FIGS. **2A** and **2B** are views illustrating manufacturing process according to the present invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIG. **2A**, on the surface of a semiconductor substrate **19**, with a first conductivity type, having field oxide layer **21** formed thereon, a first insulation layer **23**, a first conductive layer **25**, a second insulation layer **27**, a second conductive layer **29** and a third insulation layer **31** are consecutively deposited. Here, the first conductive layer **25** is the bit line, and the second conductive layer **29** is aluminum wiring containing silicon of about 1% and copper of about 0.5%. The wiring is composed of the second conductive layer, and another wiring are contacted through the contact hole **33**. Then, oxygen plasma ashing is performed to remove a remaining photoresist (not shown) positioned on top surface of the third insulation layer **31**. At this time, the process conditions are 500 SCCM (Standard Cubic Centimeter) of oxygen gas, 4–5 Torr of the pressure and 250° C.–350° C. for the temperature of the substrate. As a result, the photoresist is removed, and simultaneously the exposed wiring surface through the contact hole **33**

is oxidized, thereby forming aluminum oxide layer ($Al_2O_3$) **35** with the thickness of 30Å–80Å. The aluminum oxide layer **35**, an insulation layer, prevents reaction between the wiring, an organic solvent and water in subsequent processing to remove the photoresist, in other words, the dipping in the organic solvent and rinse, etc., Because of the above result, the wiring is protected and not damaged. After removing all the remaining photoresist on the third insulation layer **31**, to form a low resistance contact between the underlying layer wiring and the overlying layer wiring, the aluminum oxide layer **35** is subjected to an ordinary argon sputtering etching.

As shown in FIG. 2B, an overlying layer wiring **37** is formed by patterning after depositing a third conductive layer of aluminum alloy containing a get amount of copper. Here, the third conductive layer has better step coverage because the underlying layer wiring is undamaged. Accordingly, the contact area between the underlying layer wiring and the overlying layer wiring is maximized, achieving a low resistance contact.

As described above, in the method for forming the multilayer wiring according to the present invention, a protective layer of oxide layer is simultaneously coated on the top exposed surface of the underlying layer wiring, through the contact hole, with removing of the photoresist by photoresist ashing process. Therefore, the damage of the surface of wiring due to chemical reaction of an organic solvent and water in the subsequent process, is prevented so that the underlying layer wiring having better step coverage can be formed. As a result two wiring layers are interconnected with minimum contact resistance drastically enhancing electrode characteristics between the two wiring layers. Accordingly, high-density and high-speed semiconductor integrated circuit having the improved reliability can be obtained.

While the invention has been particularly shown and described with the reference to the preferred embodiment of the present invention thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and details may be made without departing from the spirit and scope of the present invention.

What is claimed is:

**1**. A method for forming multilayer wiring in a semiconductor device, said semiconductor device comprising a semiconductor substrate and insulation layers and conductive layers formed over a top surface of said semiconductor substrate, said method comprising the steps of:

forming a contact hole by selectively etching out a region of an insulation layer disposed on a first conductive layer using a photoresist pattern to thereby expose a top surface of said first conductive layer;

removing said photoresist pattern positioned on said insulation layer by plasma etching simultaneously forming a protective oxide layer on the exposed top surface of said first conductive layer; and

removing said oxide layer before forming a second conductive layer on said exposed top surface of said first conductive layer.

**2**. The method as claimed in claim **1**, wherein said first conductive layer is aluminum.

**3**. The method as claimed in claim **2**, wherein during said plasma ashing, said semiconductor substrate is heated to a temperature of 250°C.–350°C. in a reaction room having an oxygen atmosphere at a pressure of 4-5 Torr.

**4**. The method as claimed in claim **1**, wherein said oxide layer is aluminum oxide layer and has a thickness of 30Å–80Å.

**5**. The method as claimed in claim **1**, wherein said oxide layer is removed by argon sputtering etching.

**6**. The method as claimed in claim **1**, wherein said plasma etching is performed in 500 SCCM of oxygen gas and at a pressure of 4–5 Torr.

**7**. The method as claimed in claim **6**, wherein during said plasma ashing a temperature of said semiconductor substrate is 250°–350° C.

**8**. A method for forming an electrical connection on a semiconductor substrate between a first conductive layer and a second conductive layer through an intervening insulation layer formed over said first conductive layer, said method comprising the steps of:

forming a photoresist pattern on said insulation layer;

after forming said photoresist pattern, forming a contact hole by selectively etching out exposed regions of said insulation layer to expose a top surface of said first conductive layer;

removing remaining photoresist positioned on said insulation layer by plasma ashing to simultaneously form a protective oxide layer on said exposed top surface of said first conductive layer; and

removing said oxide layer before forming said second conductive layer on said exposed top surface of said first conductive layer.

**9**. The method as claimed in claim **8**, wherein said plasma ashing is performed in 500 SCCM of oxygen gas and at a pressure of 4–5 Torr.

**10**. The method as claimed in claim **9**, wherein during said plasma ashing a temperature of said semiconductor substrate is 250°–350° C.

**11**. The method as claimed in claim **8**, wherein said first conductive layer is mostly aluminum.

**12**. The method as claimed in claim **8**, wherein said first conductive layer is aluminum containing approximately one percent silicon and approximately one half percent copper.

**13**. The method as claimed in claim **8**, wherein said protective layer is an aluminum oxide layer.

**14**. The method as claimed in claim **13**, wherein said protective layer has a thickness of 30Å–80Å.

**15**. The method as claimed in claim **8**, wherein said protective layer is removed by argon sputtering etching.

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UNITED STATES PATENT AND TRADEMARK OFFICE

# CERTIFICATE OF CORRECTION

PATENT NO. : 5,252,177
DATED : October 12, 1993
INVENTOR(S) : Jong-Seo Hong

It is certified that error appears in the above-indentified patent and that said Letters Patent is hereby corrected as shown below:

Column 2, Line 9, Change "interior" to --inferior-- .

Signed and Sealed this

Nineteenth Day of September, 1995

*Attest:*

BRUCE LEHMAN

*Attesting Officer*

*Commissioner of Patents and Trademarks*